MALAYSIA-JAPAN INTERNATIONAL INSTITUTE OF TECHNOLOGY

(DEPARTMENT OF ELECTRONIC SYSTEMS ENGINEERING)

LABORATORY SHEET

ELECTRONIC ENGINEERING LABORATORY I

(SMJE 1062)

DIGITAL ELECTRONICS

NAME	:	
IC. NO	:	
YEAR / COURSE	:	
STUDENT'S SECTION	:	
LECTURER'S NAME	:	
DATE	:	

LAB 1

BASIC LOGIC GATES

Experiment 1 : NOR Gate Circuit

Experiment 2 : NAND Gate Circuit

Experiment 3 : XOR Gate Circuit

Experiment 4 : AND-OR-INVERT (A-O-I) Gate Circuit

REMINDER

It is highly recommended that students read this instruction sheet PRIOR going into the lab to ensure a smooth and proper execution of the experiments.

All records of result and observation must be filled in the result sheet must be verified by lab facilitator/ lab assistant/ lecturer.

Short reports must consist of results and discussion which has to be submitted at the end of the lab session.

Experiment 1: NOR GATE CIRCUIT

OBJECTIVE
Understanding how to construct combinational logic gates using NOR gates

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34001

PROCEDURES

All procedures in this experiment refers to **block a** in the Module KL-34001. The circuit diagram of block a is illustrated in **Figure 1**

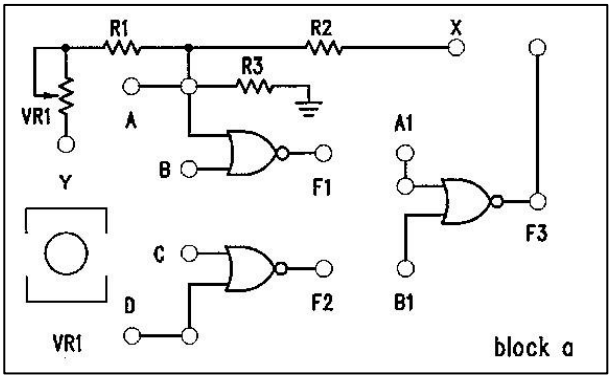


Figure 1

1.1 Use NOR gates in **block a** to construct NOT gate circuits as shown in Figure 1.1(a) & (b).

(a) **(b)**

Figure 1.1

1.1.1 To construct the circuit shown in **Figure 1.1(a)** on **block a**, connect inputs A and B to Data Switches SW0 and SW1 respectively. Then connect output F1 to Logic Indicator L1. Refer to **Figure 1.1.1**. Set SW1 (input B) to "0" and observe the states of F1 as SW0 toggles between 0 and 1. Record your observation in a truth table labelled as **Table 1.1(a)**. Does the circuit act as a NOT gate? Discuss your result.

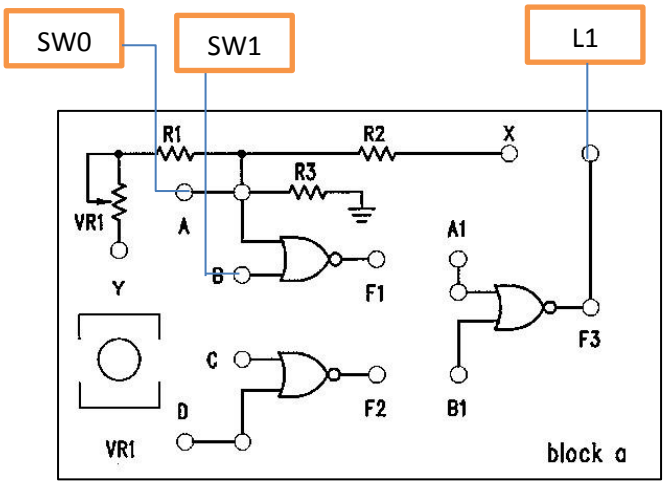


Figure 1.1.1

1.1.2 To construct the circuit shown in **Figure 1.1(b)**, connect input A to input B by using a jumper. Then connect input A to SW0 and F1 to logic indicator L1. Refer to **Figure 1.1.2.**What is the state of F1 when SW=0 and SW0=1? Record your observation in a truth table labelled as **Table 1.1(b)**. Does the circuit act as a NOT gate? Discuss your result.

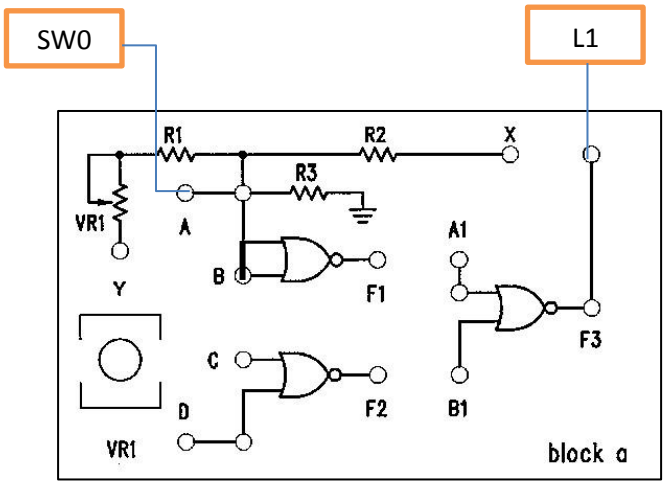
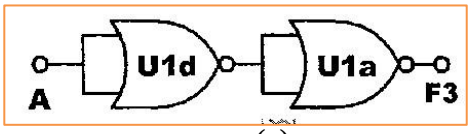
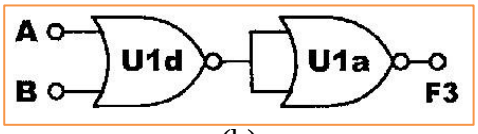


Fig. 1.1.2

1.2 Use NOR gates and jumpers in **block a** to construct gate circuits as shown in Figure 1.2 (a) & (b).



(a)



(b)

Figure 1.2

1.2.1 To construct circuit in **Figure 1.2 (a)**, use jumper to make connections between A and B, F1 and A1, A1 and B1, as illustrated in **Figure 1.2.1.** Record your result in a table and label it as **Table 1.2(a)**.

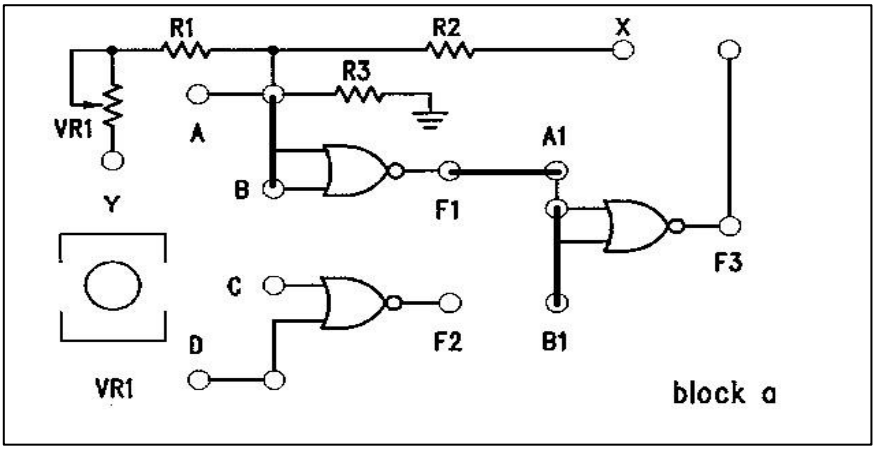


Figure 1.2.1

1.2.2 To construct circuit in **Figure 1.2 (b)**, from the previous connections you have made as shown in Figure 1.2.1 modify the connections so that A is connected to SW0 and B is connected to SW1. Record your result in a table and label it as **Table 1.2(b)**.

1.3 Use jumpers to construct the circuit as in Figure 1.3. Connect A to SW0, D to SW1 and F3 to L1. Record your result for all possible input combinations at SW0 and SW1 in Table 1.3.

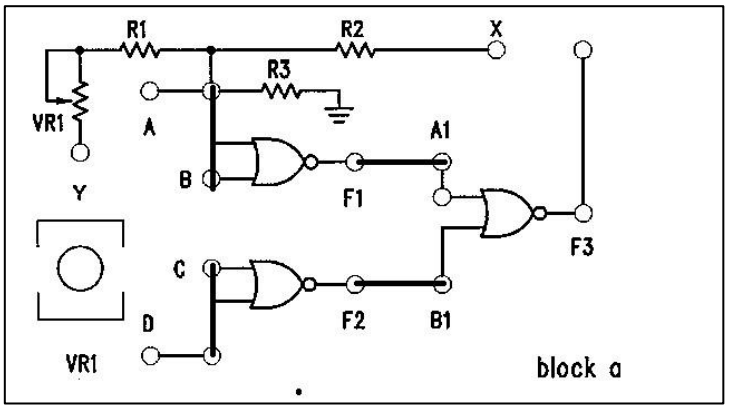


Figure 1.3

Experiment 2 : NAND GATE CIRCUIT

OBJECTIVE
Understanding how to construct combinational logic gates using NAND gates

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34001

PROCEDURES

All procedures in this experiment refer to **block c** in the Module KL-34001. The circuit diagram of block c is illustrated in **Figure 2**.

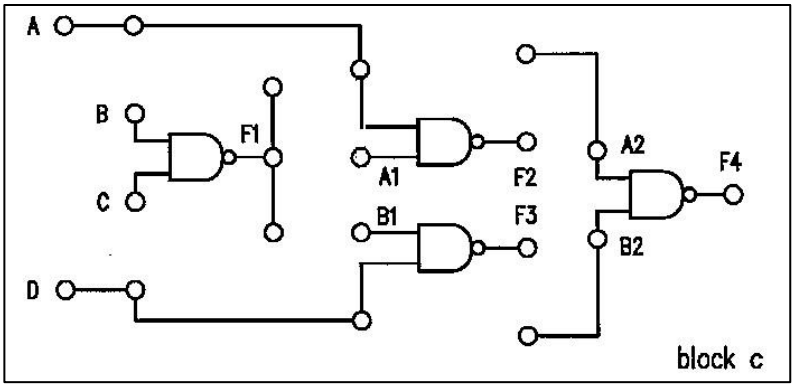
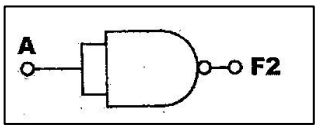
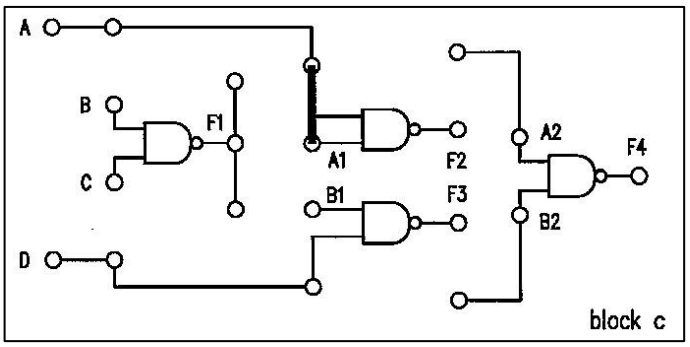


Figure 2

2.1 Construct the gate circuit shown in **Figure 2.1(a)**. Use jumper and follow the circuit connection as shown in **Figure 2.1(b)**. Connect A to SW0 and F2 to L1. Record your result in **Table 2.1**. Discuss your result.



(a)



(b)

Figure 2.1

2.2 Remove the jumper between inputs A and A1 from the previous connection made in section 2.1 (Figure 2.1). Instead, connect input **A1** to logic "1" (Vcc) by using the data switch to simulate the NAND-gate circuit illustrated in **Figure 2.2.** Observe the output state at F2, when SW0 = 0 and SW0=1. Record the observation in a truth table and label it as **Table 2.2**. Discuss your result. What does the circuit act as?

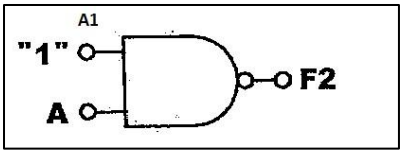


Figure 2.2

2.3 Construct the circuit as shown in **Figure 2.3**. Connect **A** to **SW0**, **A1** to **SW1** and **F4** to **L1**.

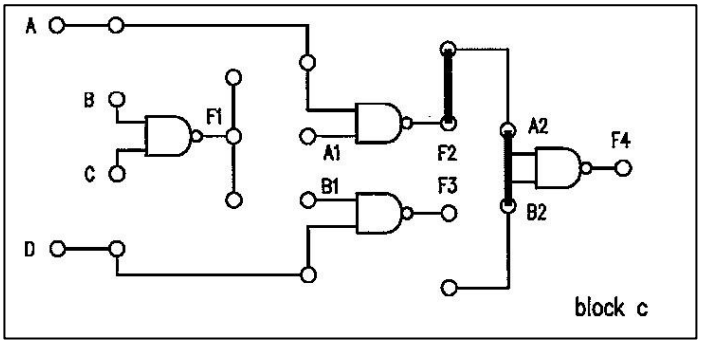
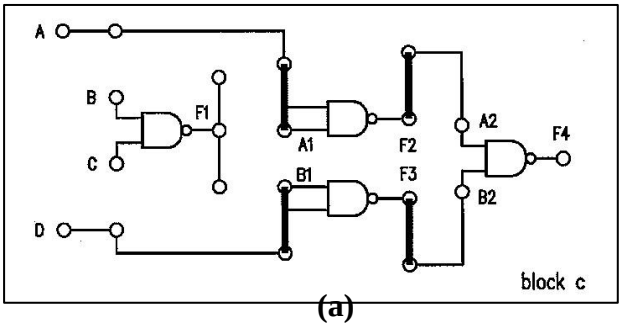


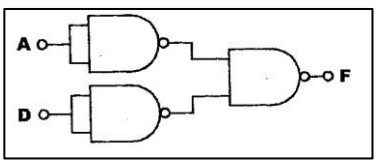
Figure 2.3

Observe the output state at F4 for all possible input combinations of A and A1. Record your result in truth table labelled as **Table 2.3**. What logic gate does the circuit perform as? Discuss your result.

2.4 Construct the circuit as shown in **Figure 2.4(a)** so that is simulates the NAND-gate circuit as shown in **Figure 2.4(b)**. Connect **A** to **SW0**, **D** to **SW1** and **F4** to **L1**. Record your observation in a truth table. Label the table as **Table 2.4.** Discuss your result.



(a)



(b)

Figure 2.4

Experiment 4 : AND-OR-INVERT GATE CIRCUIT

OBJECTIVE
Understanding the characteristics of XOR gates

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab; Module KL-34001

PROCEDURES

(I) Constructing XOR gate with NAND gates (Module KL-34001 – block c)

Procedures in this experiment refer to **block b and block c** in the Module KL-34001. The circuit diagram of block b is illustrated in **Figure 3**.

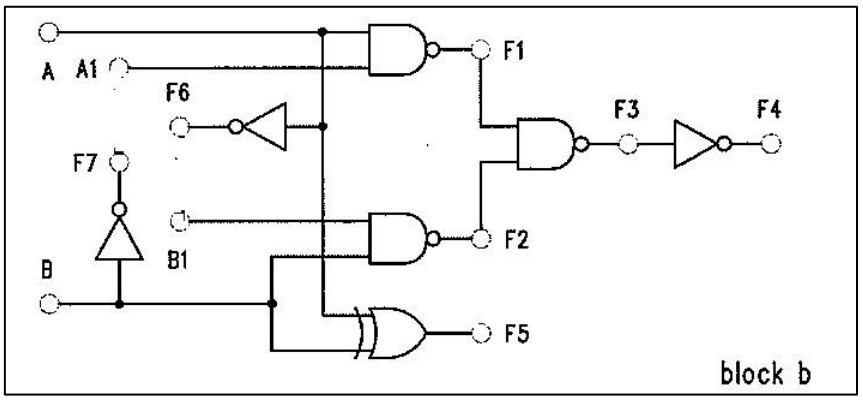


Figure 3

3.1 Construct the circuit shown in **Figure 3.1(a)** by making the necessary connections as illustrated in **Figure 3.1(b)** using the NAND-gates circuit on **block-c**. Record your result in a truth table labelled as Table 3.1. Discuss your result. In the discussion determine the Boolean expression for F1, F2, F3 and F4.

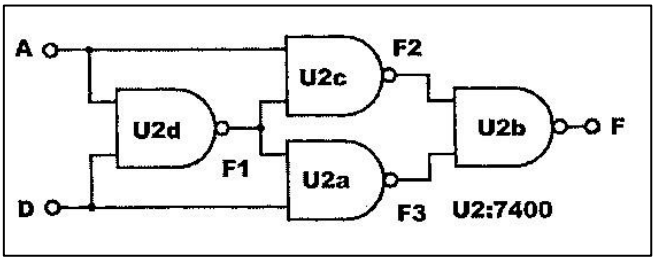


Figure 3.1 (a)

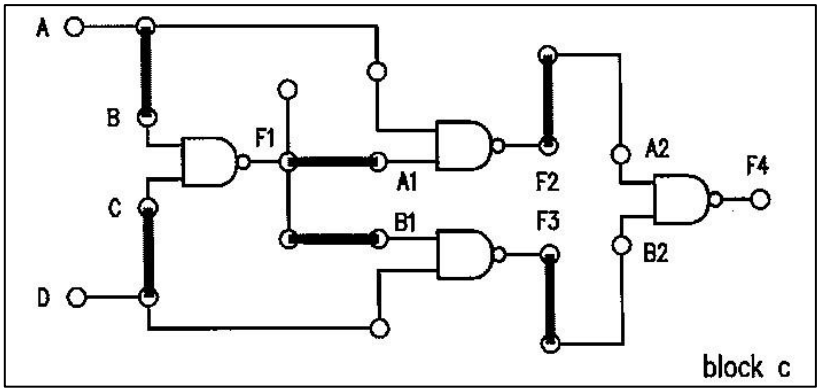


Figure 3.1(b)

3.2 Construct the circuit as shown in **Figure 3.2(a)** by following the circuit scheme illustrated in Figure 3.2 (b)using **block b** circuit module. Connect inputs **A to SW0** and **B to SW1**, outputs **F1 to L1**, **F2 to L2** and **F3 to L3**. Observe the outputs states at F1, F2, and F3 as inputs A and D change their binary combinations. Record your result in a truth table labelled as **Table 3.2**.

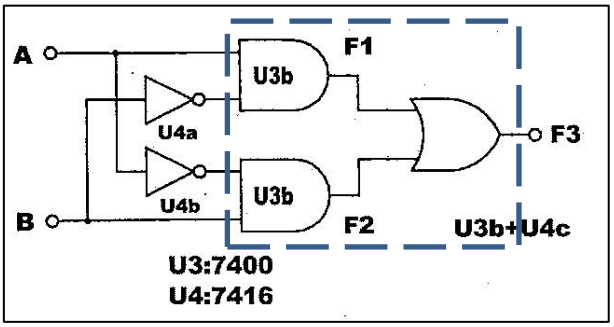


Figure 3.2(a)

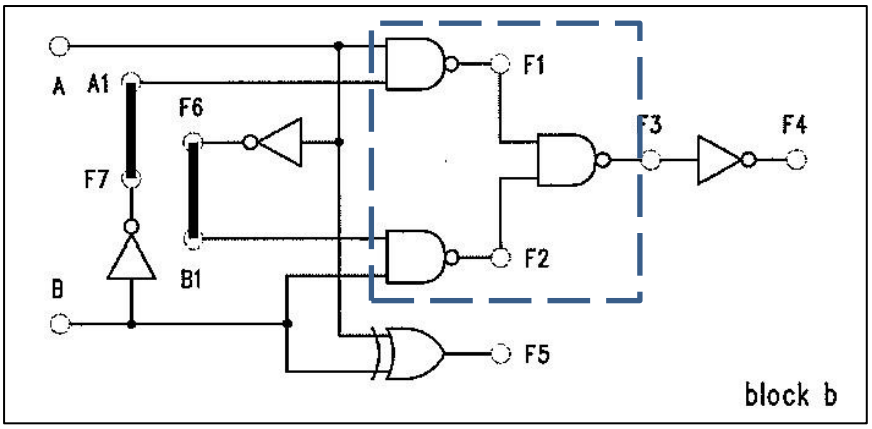


Figure 3.2(b)

Are both circuits in Figure 3.2 (a) and (b) functioning similarly? Proof your reasoning. Determine whether the combinational logic gates in the dashed rectangle box of both circuits are similar. Discuss your result and observation.

Experiment 4 : AND-OR-INVERT(A-O-I) GATE CIRCUITS

OBJECTIVE
Understanding basic principles of combined logic.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab; Module KL-34001

PROCEDURES

Procedures in this experiment refer to **block b** in the Module KL-34001.

4.1 Construct the circuit shown in **Figure 4.1(a)** by making circuit connections on **block-b** which is illustrated in **Figure 4.1(b).** Connect A, A1, B and B1 to SW0, SW1, SW2 and SW3, respectively. Connect F3 to L1 and F4 to L2.

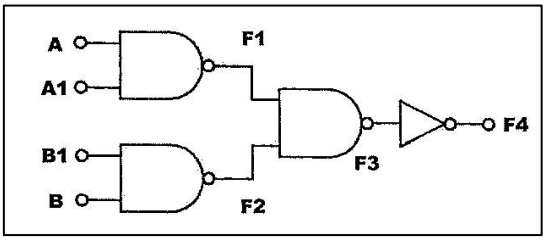


Figure 4.1(a)

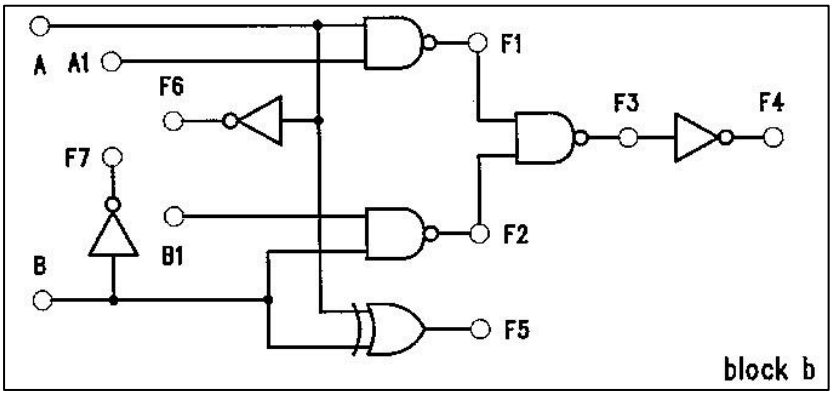


Figure 4.1(b)

4.2 (a) Set B • B1= 0. Record the output results of F3 and F4 for all input combinations of A1 and A in Table 4.2(a). Does F3 performs as an AND gate between A and A1 i.e. F3 = A • A1? Discuss your result.

(b) Set B • B1≠ 0. Record the output results of F3 and F4 for all input combinations of A1 and A in Table 4.2(b). Does F3 still perform as an AND gate between A and A1? Discuss your result.

4.3 (a) Set A • A1= 0. Record the output results of F3 and F4 for all input combinations of B1 and B in Table 4.3(a). Does F3 performs as an AND gate between B and B1 i.e. F3 = B • B1? Discuss your result.

(b) Set A • A1≠ 0. Record the output results of F3 and F4 for all input combinations of B1 and B in Table 4.3(b). Does F3 performs as an AND gate between B and B1 i.e. F3 = B • B1? Discuss your result.

4.4 Prove that the circuit in Fig 4.1(a) can be converted to AND-OR-INVERT circuit gate as shown in Figure 4.4. Show your working.

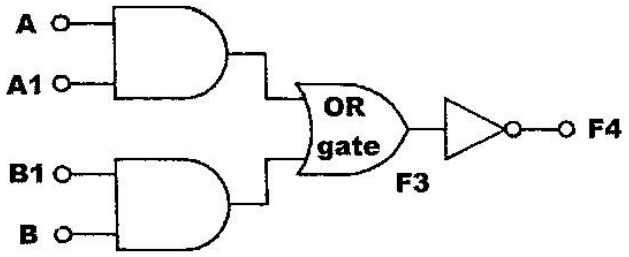


Figure 4.4

LAB 2

ARITHMETIC OPERATIONS AND CIRCUITS

Experiment 5 : Comparator Circuits

Experiment 6 : Adder Circuits

Experiment 7 : Subtractor Circuits

REMINDER

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Experiment 5: COMPARATOR CIRCUIT

OBJECTIVE
Understanding the construction and operational principles of digital comparators.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34001

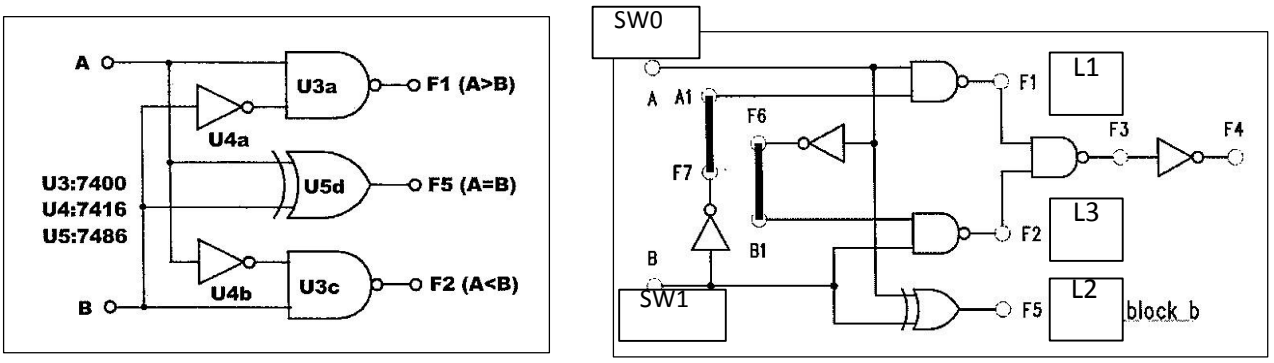
PROCEDURES

Procedures in this experiment involve **block b** and **block f** in the Module KL-34001.

(A) Comparator Circuit Constructed with Basic Logic Gates

Note : Block b circuit module is used in this part of the experiment

5.1 Figure 5.1(a) illustrates a one-bit comparator circuit. Figure 5.1 (b) illustrates the connection made on the Figure 5.1(a) using block b circuit on Lab Module KL-34001



(a) **(b)**

Figure 5.1

5.2 Connect the inputs A to SW0 and B to SW1, then connect the outputs F1, F5 and F2 to L1, L2 and L3 respectively. Enter all possible input conditions at input A and B. Record the result in **Table 5.1**. Take note of the active level of the inputs and outputs. Discuss your result.

(B) Comparator Circuit Constructed with TTL IC

Note : <u>Block f</u> circuit module is used in this part of the experiment which consists of the TTL IC 7485. The 7485 is a 4-bit comparator IC. Its pin assignment and operational table are given below.

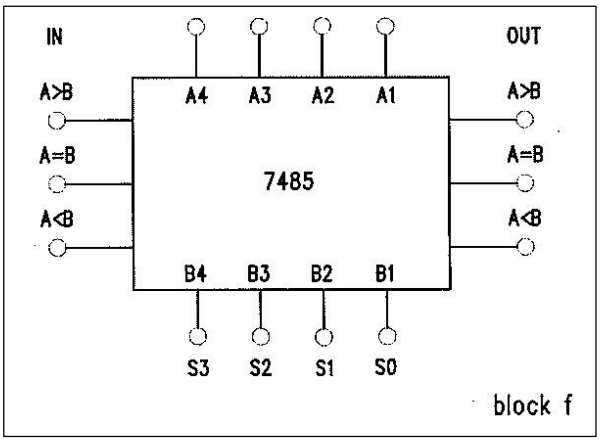


Figure 5.2(a)

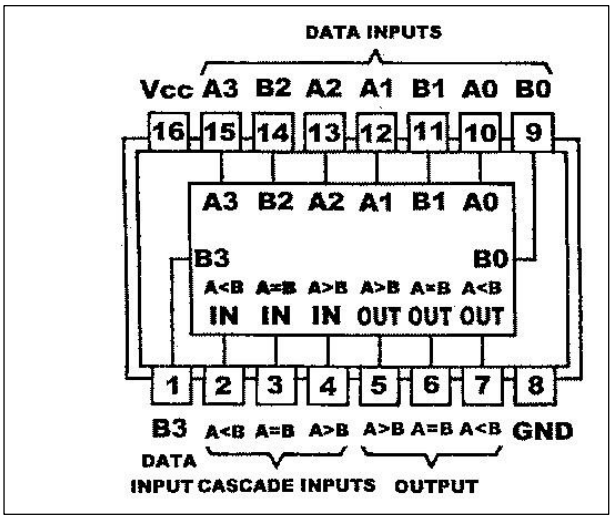


Figure 5.2 (b)

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

Figure 5.2(c)

Figure 5.2 : (a) block f (b) IC 7485 pin assignment (c) IC 7485 operational table

5.3 Do the subsequent wiring connections :

(i) Connect the cascading input pins as follows:

A>B to SW7, A=B to SW5 and A<B to SW6.

(ii) Connect the data input/ comparing input pins as follows:

A1-A4 to DP0 – DP3 of DIPA and B1-B4 to DP0 – DP3 of DIPB respectively.

(iii) Connect the output pins to light indicators

A=B to L15, A< B to L14, A > B to L13(e.g A4-A1 = 10101 and B4-B1=1010)

5.4 Define inputs A1-A4 as As and B1-B4 as Bs. Then make the value of As equal to Bs (e.g A4-A1 = 10101 and B4-B1=1010). Follow the input sequence of comparing inputs given in **Table 5.2** and record the outputs.

5.5 Connect cascading inputs A >B to "x", A < B to "0" and A=B to "1". Change the value of the As and Bs (the DIPA and DIPB switches) . Observe and record the output status under the following data/ comparing input conditions in **Table 5.3**.

(i) value of As > value of Bs

(ii) value of As < value of Bs

(iii) values of As = value of Bs

Experiment 6: ADDER CIRCUITS

OBJECTIVE
Understanding the characteristics of half-adder and full-adder in the arithmetic circuit.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34001/ kl-34002

PROCEDURES

Procedures in this experiment involve **block e** of Module KL-34001.

(A) Constructing Half-Adder with Basic Logic Gates

Note : Block e circuit module is used in this part of the experiment

6.1 Figure 6.1(a) shows a half-adder circuit. Construct the circuit using **block e** circuit module as shown in Figure 6.1(b)

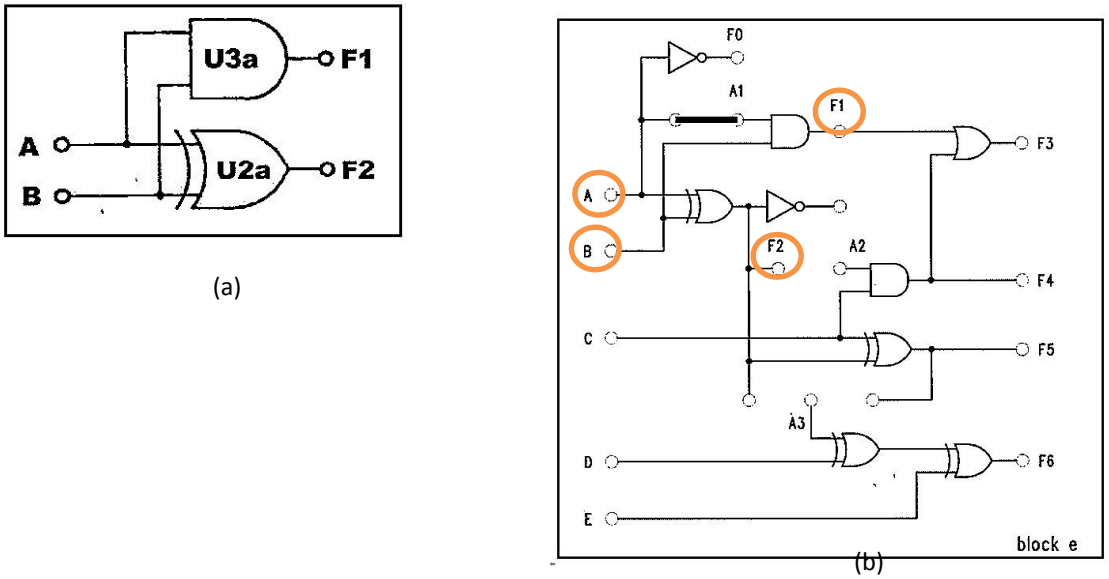
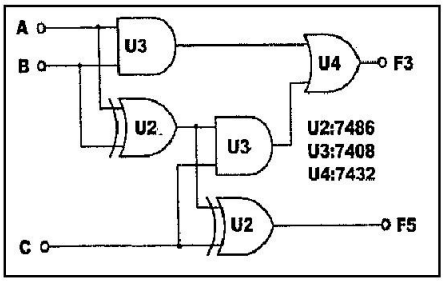


Figure 6.1

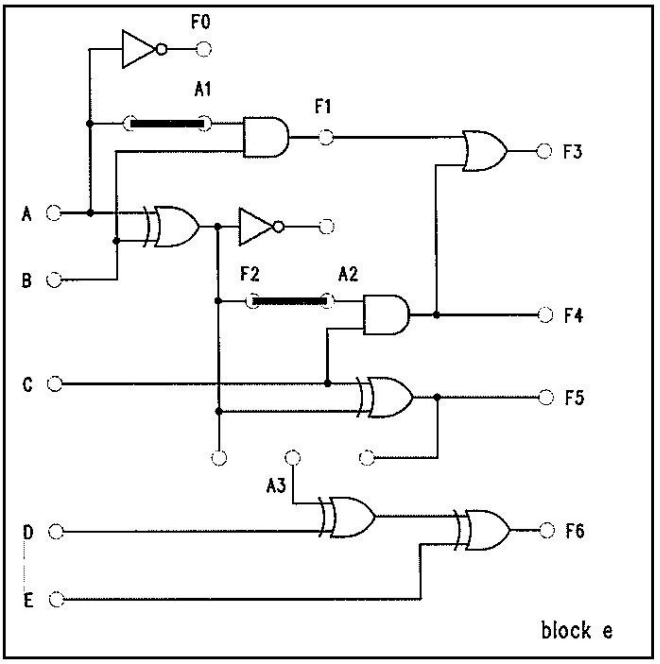
6.2 Connect inputs A to SW0 and B to SW1 as well as the outputs F1 and F2 to light indicators. Observe and record the outputs in **Table 6.1** for all possible combinations of inputs.

(B) Constructing Full-Adder with Basic Logic Gates

6.3 Figure 6.2(a) shows a full-adder circuit. Construct the circuit using **block e** circuit module as shown in Figure 6.2(b)



(a)



(b)

Figure 6.2

6.4 Connect the inputs A, B and C to switches and outputs F3 and F5 to light indicators. Enter all possible input conditions at inputs A, B and C. Record the result in **Table 5.2**. Label the inputs and the outputs. Discuss your result.

(C) Full Adder Circuit with IC

Note : <u>Block d</u> circuit on Lab Module KL34002 is used in this part of the experiment which consists of 4-bit adders IC 74HC83.

6.5 Figure 6.3 illustrates how to implement a full adder with a TTL IC74HC83. Construct the circuit as shown in Figure 6.3 to form an adder/ subtractor by making the necessary connections on the circuit **block** d at **Lab Module KL34002** so that it performs as a 4-bit full adder that adds number X ($X_3 - X_1$) and Y ($Y_3 - Y_1$).

6.6 Connect input X's and Y's to DIP switches, Y5 to a toggle switch SW0. Determine the logic level at SW0 to make the circuit a adder.

6.7 Follow input sequences in Table 6.3. Observe and record the outputs.

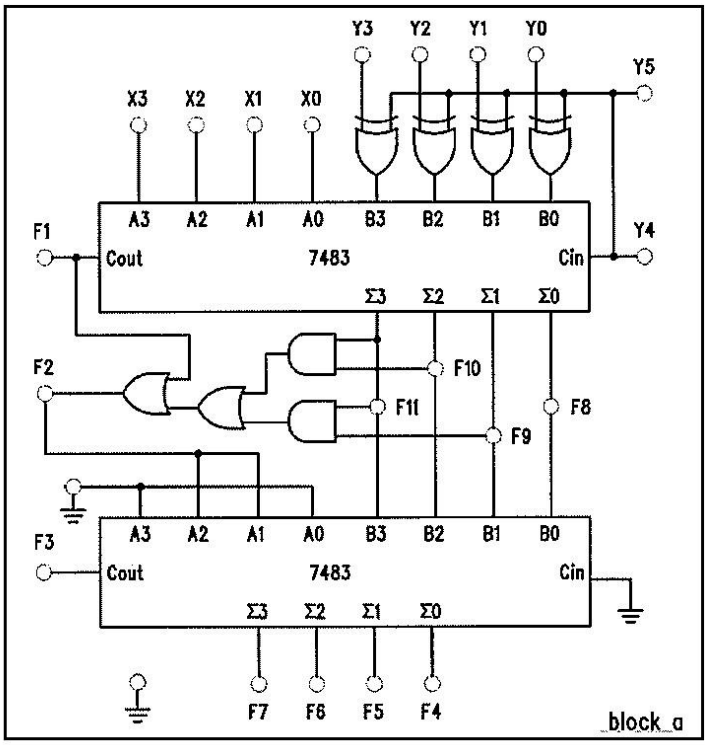

Y3
Y2
Y1
Y0
Y5
X3
X2
X1
X0
A3
A2
A1
A0
B3
B2
B1
B0
F1
Cout
7483
Cin
Y4
Σ3
Σ2
Σ1
Σ0
F2
F10
F11
F8
F9
A3
A2
A1
A0
B3
B2
B1
B0
F3
Cout
7483
Cin
Σ3
Σ2
Σ1
Σ0
F7
F6
F5
F4
block_a

Figure 6.3

Experiment 7: SUBTRACTOR CIRCUITS

OBJECTIVE
Understanding the theory of complements and construction of subtractor circuits.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34001/ kl-34002

PROCEDURES

Procedures in this experiment involve **block e** of Module KL-34001.

(A) Constructing Half-Subtractor with Basic Logic Gates

Note : Block e circuit module is used in this part of the experiment

7.1 Figure 7.1(a) shows a half-subtractor circuit that implements a half-subtractor operation described by Table 7.1(a) Make the circuit connection on block e to make it functions as half-subtractor.

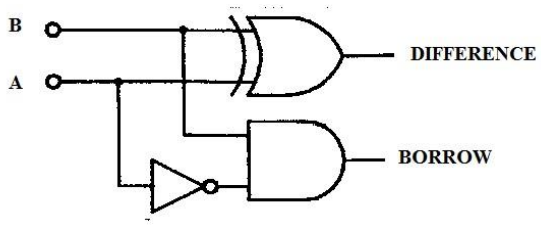


Figure 7.1 (a)

A	B	BR	DIFF
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Table 7.1(a)

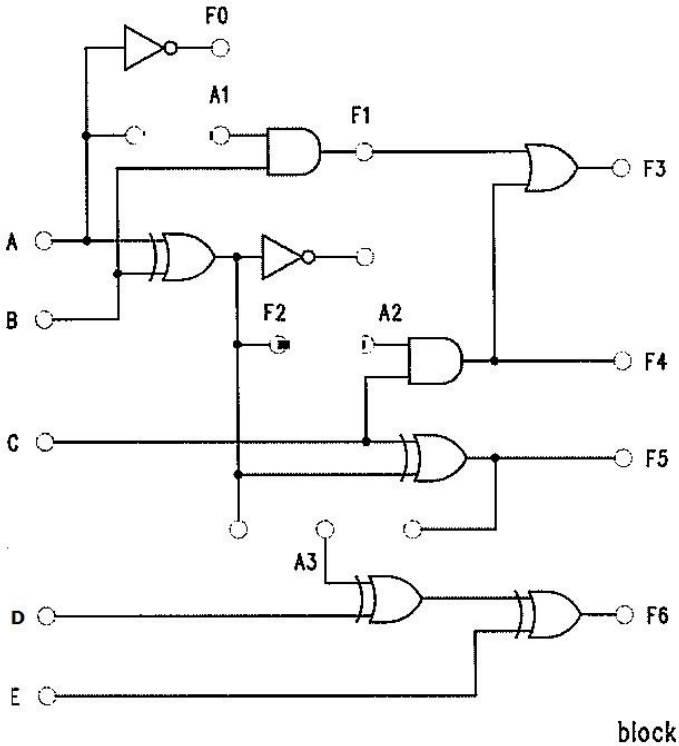


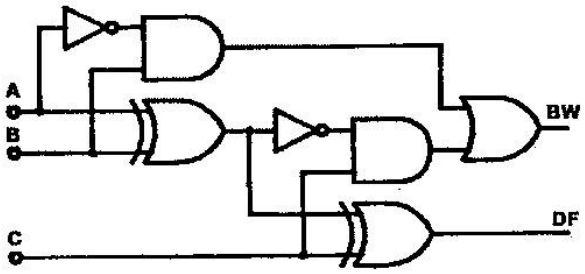
Figure 7.1 (b)

block e

7.2 Apply input signals to A and B by connecting it to SW0 and SW1 respectively. Determine the related outputs on **block e** for **DIFF** and **BR**. Observe and record the outputs by completing Table 7.1(b).

(B) Constructing Full-Subtractor with Basic Logic Gates

7.3 Figure 7.2(a) shows a full-subtractor circuit that implements a full-subtractor operation described by Table 7.2(a) Make the circuit connection on block e to make it functions as full-subtractor.



C	A	B	BR	DIFF
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Table 7.2 (a)

7.4 Apply input signals to A, B and C by connecting it to SW2, SW1 and SW0 respectively. Determine the related outputs on **block e** for DIFF and BR. Observe and record the outputs by completing Table 7.2(b).

(C) Constructing Full-Subtractor with TTL IC74HC83

7.5 Figure 7.3(a) illustrates how to implement a full subtractor with a TTL IC74HC83. Construct the circuit as shown in Figure 7.3(b) to form an adder/ subtractor by making the necessary connections on the circuit **block** d at **Lab Module KL34002** so that it performs as a 4-bit full subtractor that subtracts number X ($X_3 – X_1$) and Y ($Y_3 – Y_1$).

7.6 Connect input X's and Y's to DIP switches, Y5 to a toggle switch SW0. Determine the logic level at SW0 to make the circuit a subtractor.

7.7 Follow input sequences in Table 7.3. Observe and record the outputs.

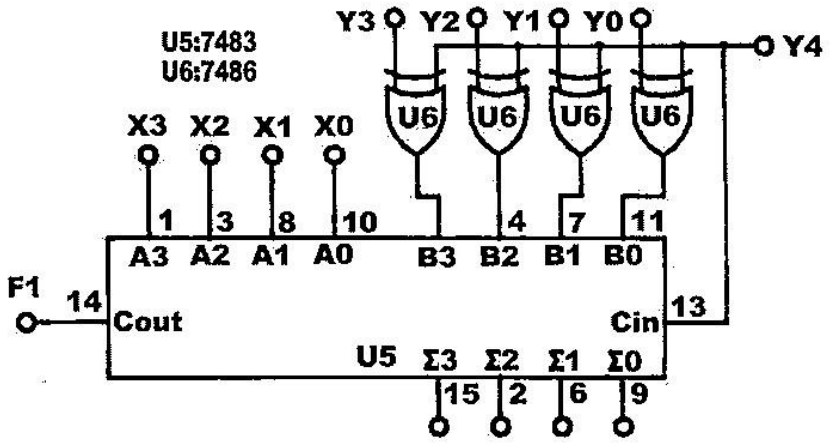


Figure 7.3(a)

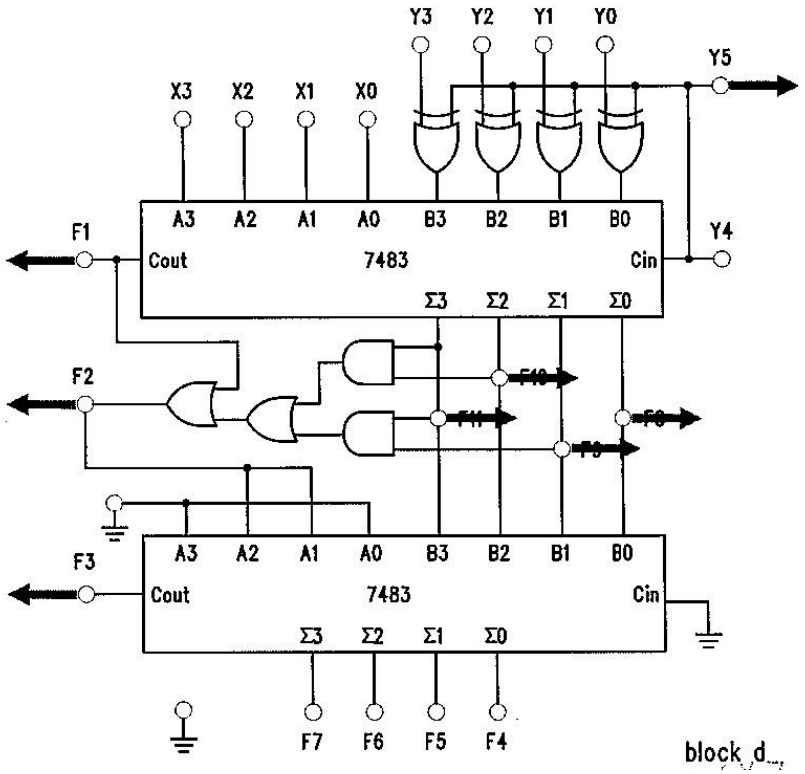


Figure 7.3(b)

LAB 3

MSI LOGIC CIRCUITS

Experiment 8 : Encoder Circuits

Experiment 9 : Decoder Circuits

Experiment 10 : Multiplexer Circuits

REMINDER

It is highly recommended that students read this instruction sheet PRIOR going into the lab to ensure a smooth and proper execution of the experiments.

All records of result and observation must be filled in the result sheets and to be verified by lab facilitator/ lab assistant/ lecturer prior leaving the lab.

Short reports must consist of results and discussion which has to be submitted at the end of the lab session.

Experiment 8: ENCODER CIRCUITS

OBJECTIVE
Understanding the operating principles of encoder circuits.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34003

PROCEDURES

(A) Constructing a 4-2 Encoder with basic logic gates (KL-34003 block e)

8.1 Construct the circuit shown in Figure 8.1. Connect inputs A ~ D to toggle switches in order and outputs F8 and F9 to logic indicators. Follow the input sequence shown in Table 8.1 of the result sheet and record the results in **Column A**..

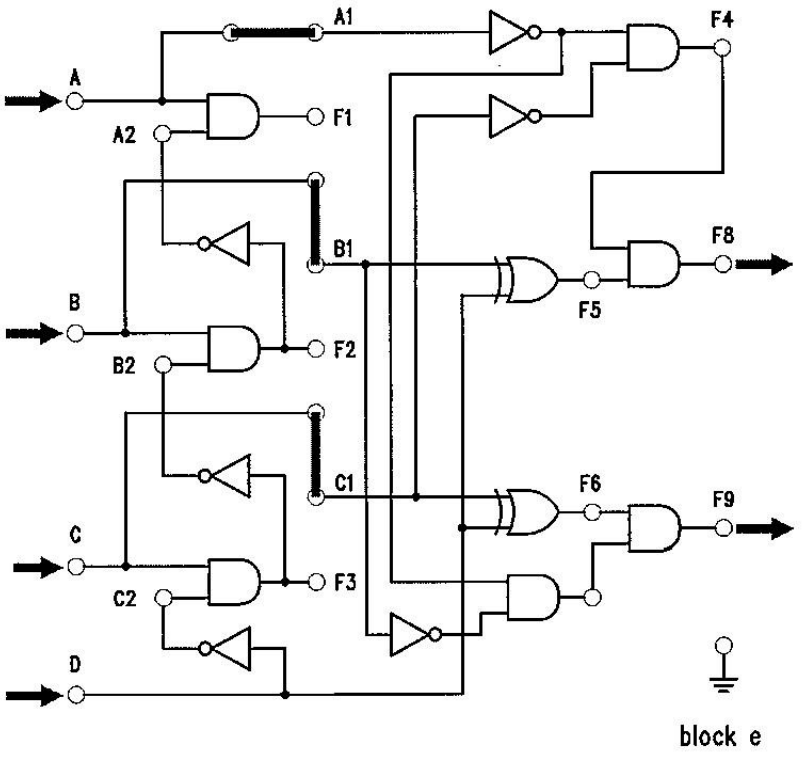


Figure 8.1

8.2 Construct the circuit shown in Figure 8.2 by making minor modification to connect point **A1 to F1**. Follow the input sequence shown in Table 8.1 of the result sheet and record the results in **column B**.

8.3 Compare the output states in Column A and B in Table 8.1. What is the difference between them? Discuss.

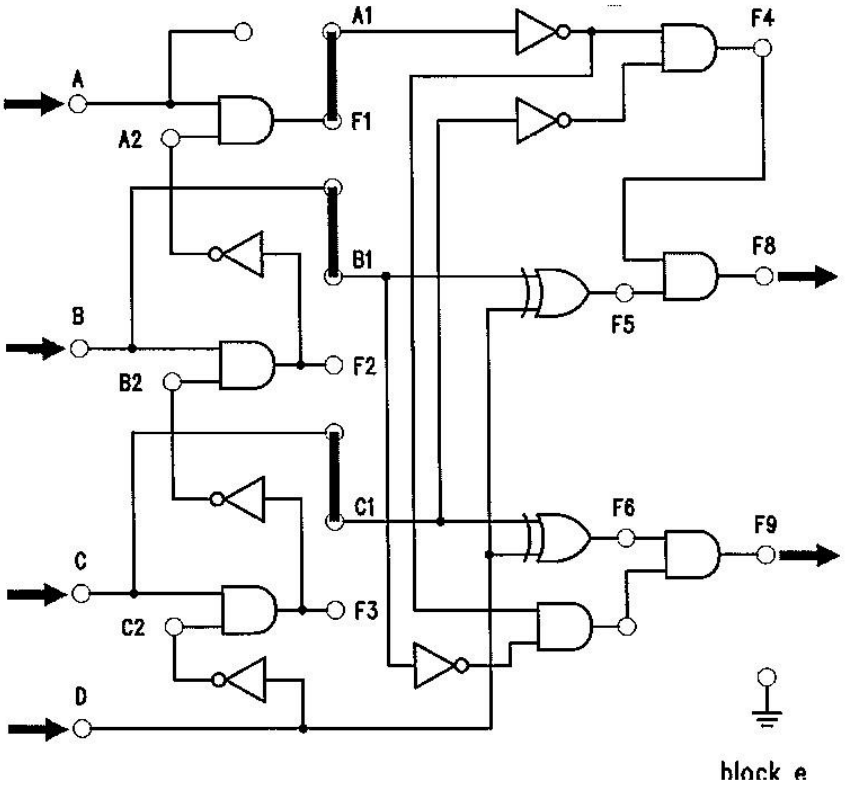
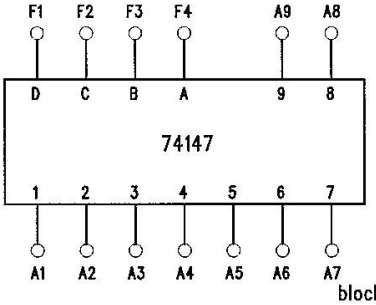


Figure 8.2

(B) Constructing a 10-4 Encoder with TTL IC 74147 (KL-34003 block a)

8.4 Use block a of Lab Module KL34003. Connect inputs A1~A9 to DIP switches. Connect outputs F1~F4 to logic indicators. Follow the input sequences given in Table 8.2 and record the output states. Discuss your results.



block a

Experiment 9: DECODER CIRCUITS

OBJECTIVE
Understanding the operating principles of decoder circuits.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34003/ KL-34001

PROCEDURES

(A) Constructing a 4-2 Decoder with basic logic gates (KL-34003 block g)

9.1 Construct the circuit shown in Figure 9.1 on **block g** of lab module KL 34003. Connect inputs A and B to toggle/ data switches and outputs F1 ~ F4 to logic indicators. Apply all possible input conditions to A and B. Record and discuss on the output results in **Table 9.1** in the result sheet.

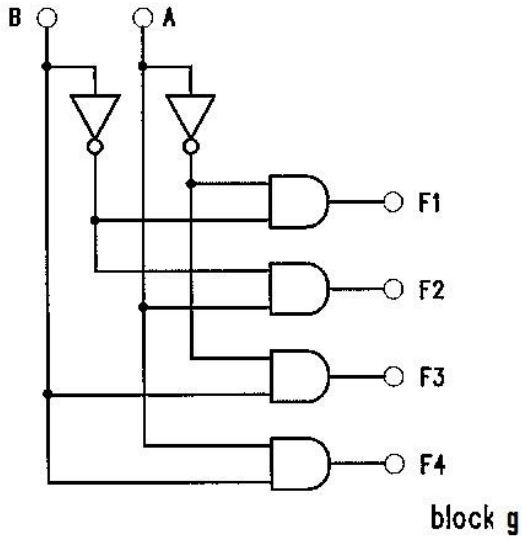


Figure 9.1

(B) Constructing a 4-to-10 Decoder with TTL IC 7442 (KL-34001 block g)

9.2 Refer to **block g** of Lab Module KL34003 as shown in Figure 9.2. Connect inputs A1, B1, C1 and D1 to data switches (SW) and outputs 0 ~ 9 to logic indicator. Set input to different values and record the output results in **Table 9.2**

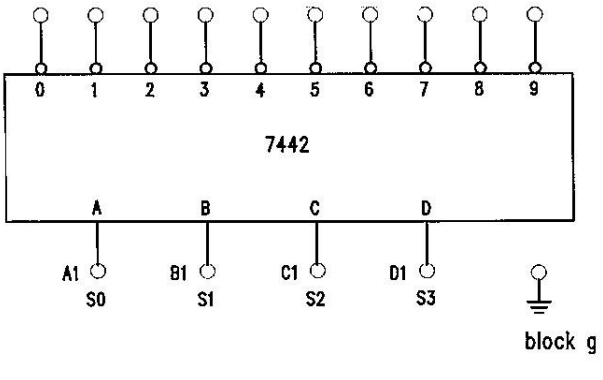
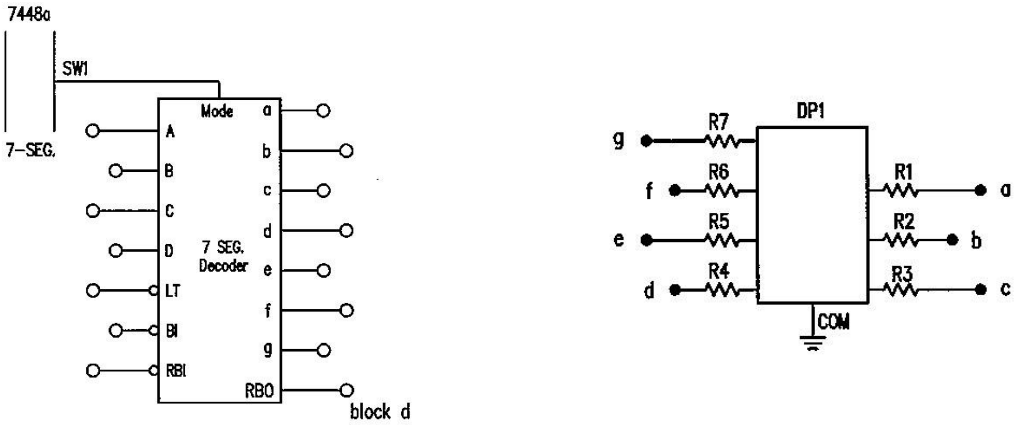


Figure 9.2

(C) BCD-to-7 Segment Decoder/ Driver (KL-34003 block d)

9.3 Figure 9.3(a) shows the decoding circuit to display 0-9 digit on 7-segment and Figure 9.3(b) illustrates the connections to be made between the 7-segment decoder/driver outputs a ~ g and the common cathode 7-segment display.



(a) (b)

Figure 9.3 : 7-segment display decoding circuit

9.4 **Table 9.3** is a functional table of the 7-segment decoder TTL IC 7448a and Figure 9.4 illustrates the display. **Table 9.4** is a functional table of a 7-segment decoder implemented using CPLD. Notice the difference?

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI	OUTPUTS							RBO
	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}$	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	H
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	H
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	H
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	H
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	H
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	H
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	H
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	H
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	H
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	H
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	H
BI	X	X	H	L	H	L	L	L	L	L	L	L	L	L	H
RBI	H	L	H	L	H	H	H	L	L	L	L	L	L	L	L
LT	L	X	H	H	L	L	H	H	H	H	H	H	H	H	H

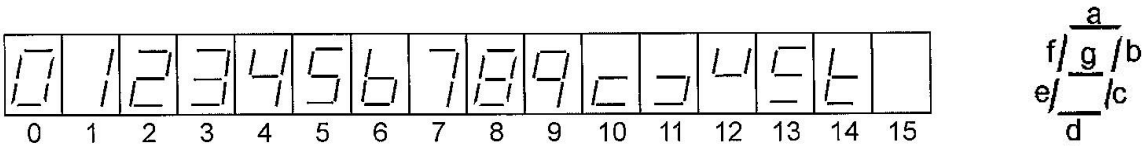


Figure 9.4 : 7-segment display implemented by IC7448a

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI	OUTPUTS							RBO	Display
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g		
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	H	0
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	H	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	H	2
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	H	3
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	H	4
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	H	5
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	H	6
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	H	7
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	H	8
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	H	9
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	H	A
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	H	b
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	H	C
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	H	D
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	H	E
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	H	F
BI	X	X	H	L	H	L	L	L	L	L	L	L	L	L	H	X
RBI	H	L	H	L	H	H	H	L	L	L	L	L	L	L	L	X
LT	L	X	H	H	L	L	H	H	H	H	H	H	H	H	H	X

Table 9.4 : 7-segment decoder functional table implemented by CPLD

9.5 (i) Refer to block d of module KL-34003. Connect inputs D, C, B, A to data switches in the correct order of msb ~ lsb. Connect display control inputs LT (Lamp Test), BI (Blanking Input) and RBI to data switches and output RBO to logic indicator. Set all the display control inputs LT, BI and RBO to HIGH. Set the IC 7448 to function.

(ii) Follow the input sequence shown in Table 9.5 in the result sheet. Observe the outputs of the 7-segment display and output RB0, and record the results in **Table 9.5**.

Table 9.3 : 7-segment display decoder (IC7448) functional table

9.6 Now set control inputs LT=HIGH , BI = HIGH and RBI = LOW. Follow the input sequence shown in Table 9.5 in the result sheet. Observe the outputs of the 7-segment display and output RB0, and record the results in **Table 9.6 (a)**.

9.7 Now set control inputs LT= LOW, BI = HIGH and RBI = HIGH. What does the display show? Observe and record your output results for a few random data input D~A in **Table 9.6(b)**.

9.8 Now set control inputs LT= HIGH, BI = LOW and RBI = LOW. What does the display show? Observe and record your output results for a few random data input D~A in **Table 9.6(c)**.

9.9 Compare the output results of Table 9.5 and Table 9.6(a) (b) (c) and discuss.

Figure 10.2

Experiment 10: MULTIPLEXER CIRCUITS

OBJECTIVE
Understanding the operating principles and construction of multiplexer circuits.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34003

PROCEDURES

(A) Constructing a 2-to-1 Multuplexer with basic logic gates (KL-34003 block g)

10.1 Construct the circuit shown in Figure10.1 on **block f** of lab module KL 34003. Connect data inputs A and B as well as selector C to toggle/ data switches (SW) and output F3 to logic indicator. Apply all possible input conditions to C, B and A in order as in Table 9.1. Record and discuss on the output results in the result sheet.

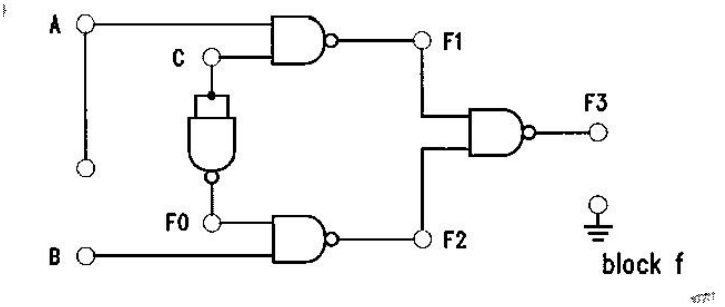


Figure 10.1

(B) Creating function using Multiplexer IC TTL 74151 (KL-34003 block c)

10.2 Refer to **block c** of Lab Module KL34003. Construct the circuit as shown in Figure 10.2 which is described by the function :F (D, C, B, A) = ∑ (0, 2, 4, 5, 7, 8, 10, 11, 15)

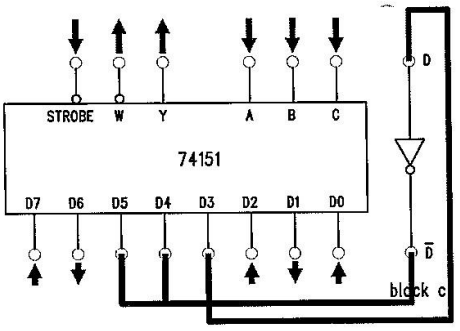


Figure 10.2

10.3 As the Figure 10.2(b), connect D4 abd D5 to $\overline{D}$, D3 to D. Connect D0, D2, D7 to SW7 and then switch to HI. Connect D1 and D6 to GND (on block e). Since D, C, B, A has 16 possible variations but the 74151 has only 8 variations, connect inputs D, C, B, and A to SW3, SW2, SW1 and SW0, respectively. Connect STROBE to ground and Y to L0.

$\overline{D}$	0	1	2	3	4	5	6	7
D	8	9	10	11	12	13	14	15

Figure 10.2(b)

10.4 Varying DCBA from 0000 to 1111 in order, and see if Y operates only when DCBA is 0, 2, 4, 5, 8, 10, 11 and 15.

10.5 With a complete circuit, fill up Table 10.2 and compare whether the table is similar to the function given.

(C) Constructing a 8-to-1 Multiplexer circuit with TTL IC 74151 (KL-34003 block c)

10.6 Refer to block c of Module KL34003 as shown in Figure 10.3. Connect inputs D7 ~ D0 to DIP switch, select inputs C, B and A to data switches and outputs W and Y to logic indicator. Connect STROBE input to data switch and then set to LOW. Set the DIP switches at random.

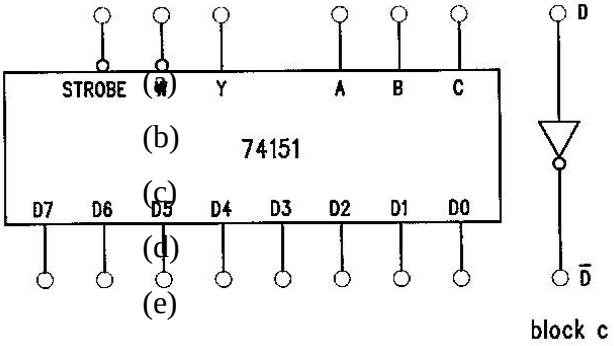


Figure 10.3

Electronic Engineering Laboratory 1

SMJE 1062

LAB 4

SEQUENTIAL LOGIC CIRCUITS

Experiment 1: **R-S and D Flip-flops**

Experiment 2: **J-K Flip-flops and**
Master-Slave J-K Flip-Flop

Experiment 3: **Shift Register with D Flip-Flops**

Experiment 4: **Preset Left/Right Register**

Experiment 1: R-S and D Flip-Flops

OBJECTIVE
Understanding how to construct R-S and D flip-flops using basic logic gates

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34004.

PROCEDURES

All procedures in this experiment refers to **block a** in the Module KL-34004.

1. Make connections as indicated in **Figure 1.2** on block a, to construct the circuit shown in **Figure 1.1.**

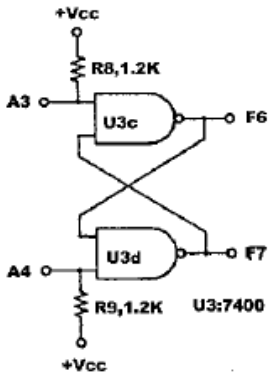


Figure 1.1: R-S Flip-Flop

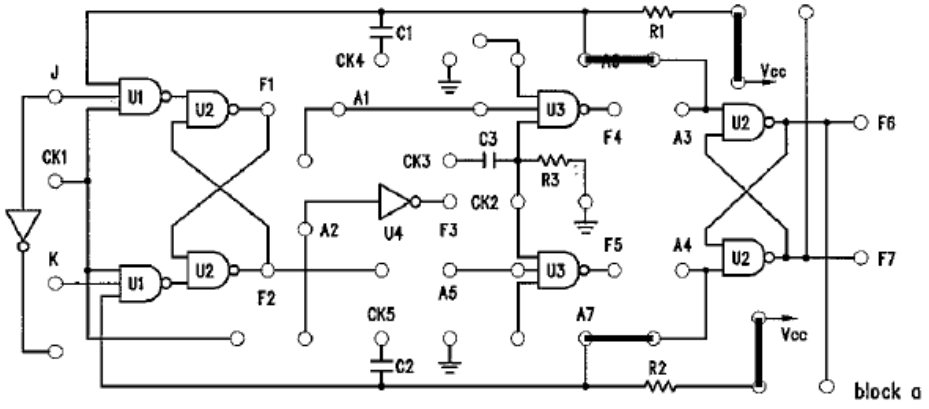


Figure 1.2: Block a of Module KL-34004

2. Connect A3 and A4 to the $\bar{A}$ of PULSE A and the $\bar{B}$ of PULSE B separately. Connect F6 to L0 indicator, F7 to L1 indicator. Observe the output states of F6 and F7 when A3 and A4 have not been triggered. Then, restart the POWER and observe the output states of F6 and F7. Discuss your observation.
3. Follow and apply the inputs in **Table 1.1**, and record the corresponding results of F6 and F7.

Sequence	Input A4	Input A3	Output F7	Output F6
0	0	0		
1	0	⊓		
2	⊓	0		
3	⊓	⊓		

Table 1.1

4. Follow the scheme of **Figure 1.3**, use jumpers to construct the circuit of **Figure 1.4**. Connect CK2 to SW0.

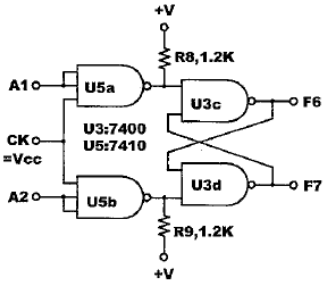


Figure 1.3 R-S clock Flip-Flop

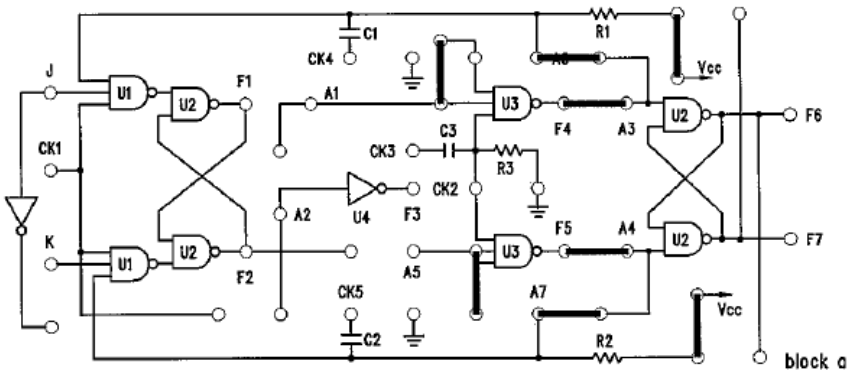


Figure 1.4 Block a of Module KL-34004

5. Connect A1 to A of PULSE A, A5 to B of PULSE B. Set CK2 to 1. Apply the inputs sequences of A1 and A5 in **Table 1.2**, and record the corresponding results. Discuss your observation.

Sequence	Input A5	Input A1	Output F7	Output F6
0	0	0		
1	0	⎍		
2	⎍	0		
3	⎍	⎍		

Table 1.2

6. Construct D flip-flop with R-S flip-flops by following the scheme of **Figure 1.5**. Use jumpers to construct the circuit of **Figure 1.6**.

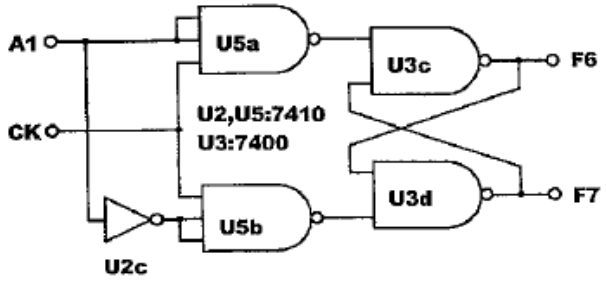


Figure 1.5

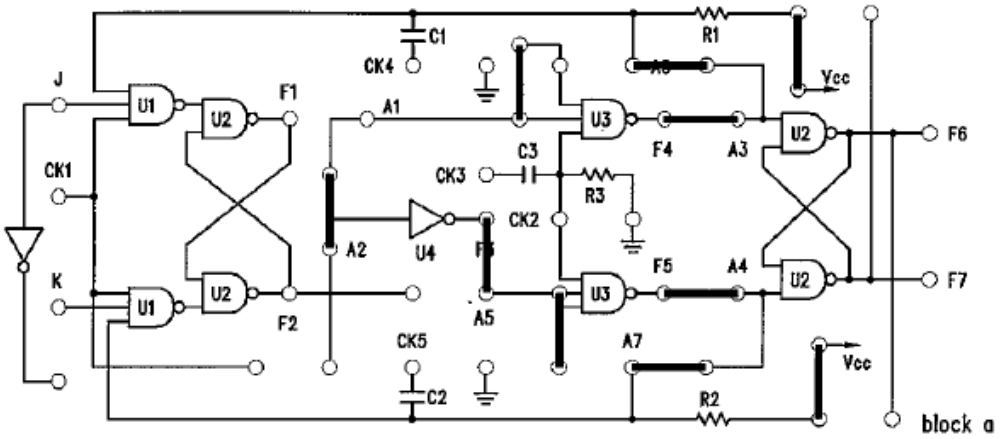


Figure 1.6

7. Connect A1 to SW1, CK2 to A of PULSE A. Connect output F6 to L0 indicator. Apply the inputs sequences in **Table 1.3**, and record the corresponding results. Discuss your observation.

CK2	A1	F6
0	0	
0	1	
⎍	0	
⎍	1	

Table 1.3

Experiment 2: J-K Flip-flops and Master Slave J-K Flip-flops

OBJECTIVE

Understanding how to construct J-K Flip-flop with D Flip-flops and Master Slave J-K Flip-flops

EQUIPMENTS REQUIRED

KL-32001 Advanced Digital Logic Lab ; Module KL-34004.

PROCEDURES

All procedures in this experiment refers to **block a** in the Module KL-34004.

1. To construct the circuit shown in **Figure 2.1**, make connections as indicated in **Figure 2.2** on block a. Connect CK2 to A of PULSE A, A1 to SW0, A5 to SW1 and F6 to L1.

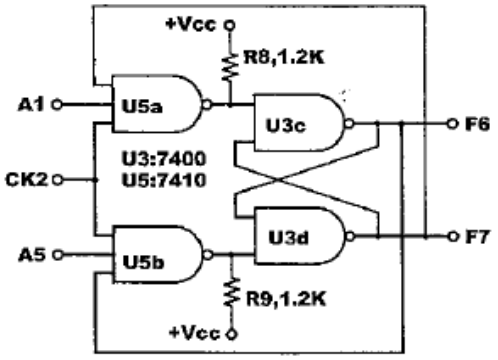


Figure 2.1

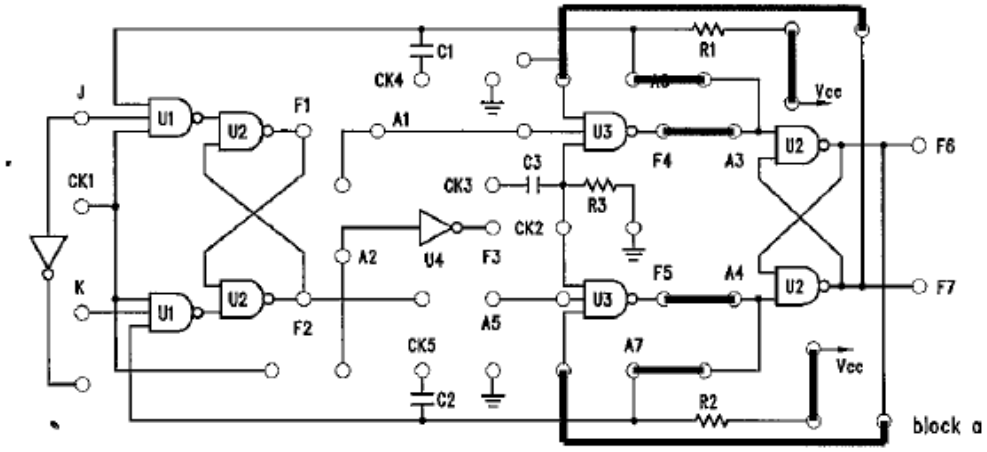


Figure 2.2

2. Apply the input sequences in **Table 2.1**, and record the corresponding results. Discuss your results.

CK	Input A5	Input A1	Output F6
⎍	0	0	
⎍	0	1	
⎍	1	0	
⎍	1	1	
⎍	1	1	
⎍	1	1	

Table 2.1

3. Construct a Master-Slave J-K Flip-flops with dual R-S Flip-flops by following the scheme of **Figure 2.3**. Use jumpers to construct the circuit of **Figure 2.4**. Connect J to SW1, K to SW0, CK1 to SW2, F1 to L3, F2 to L2, F6 to L1 and F7 to L0.

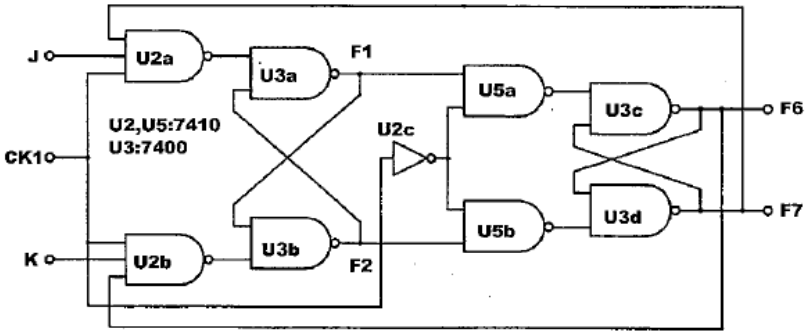


Figure 2.3

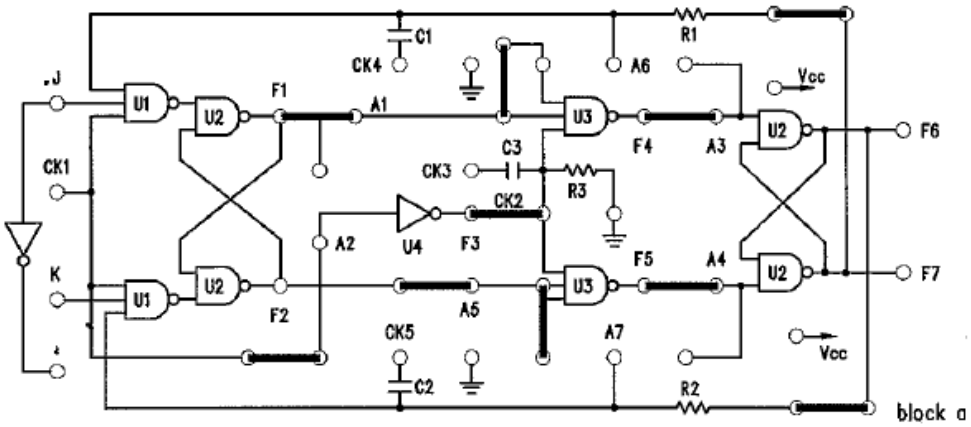


Figure 2.4

4. Measure the signals of CK1, F1, F2, F6 and F7, and record the results in **Table 2.3**.

CK1	J	K	F1	F2	F6	F7
⎍	**0**	**0**				
0 ➡ 1	**1**	**0**				
1 ➡ 0	**1**	**0**				
0 ➡ 1	**0**	**1**				
1 ➡ 0	**0**	**1**				
0 ➡ 1	**1**	**1**				
1 ➡ 0	**1**	**1**				
0 ➡ 1	**1**	**1**				
1 ➡ 0	**1**	**1**				

Table 2.3

Experiment 3: Shift Register with D Flip-flops

OBJECTIVE
Understanding how to construct shift register with D Flip-flops

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34004.

PROCEDURES

All procedures in this experiment refers to **block b** in the Module KL-34004.

1. As shown in **Figure 3.1**, a shift register can be implemented with four D flip-flops, which is like the four-bit shift register "74273".

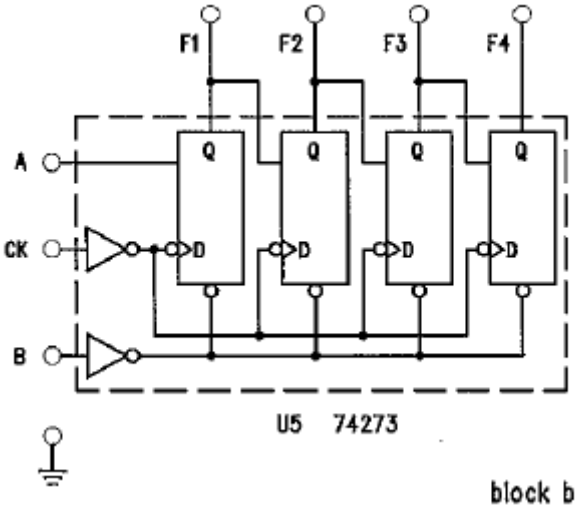


Figure 3.1

2. Connect B(Clear) to SW0, A(I/P) to SW1, CK to the A of Pulse A, F1 to L4, F2 to L3, F3 to L2 and F4 to L1.
3. First, set B(Clear) to LOW, and then set it to HIGH. Switch SW1 to HIGH, and switch the A of Pulse A four times, and then record the statuses of F1 to F4. Discuss you observation.
4. Set B(Clear) to LOW, and then set it to HIGH. Switch SW1 to HIGH and press down the A of Pulse A, and then set SW1 to LOW. Switch the A of Pulse A three times and observe the statuses of F1 to F4. Record your result and discuss your finding.

Experiment 4: Preset Left/Right Register

OBJECTIVE
Understanding how to construct a preset left/right register

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34004.

PROCEDURES

All procedures in this experiment refers to **block d** in the Module KL-34004.

1. **Figure 4.1** shows the block diagram of a 4-bit preset left/right register consisted of four D flip-flops. The MODE CONTROL is set LOW to control SERIAL INPUT shifting. Contrarily, the MODE CONTROLS is set HIGH to make the bits, A, B, C, and D, loaded in D flip-flops. The CLOCK1 is used for RIGHT SHIFT and the CLOCK2 is used for LEFT SHIFT. **Table 4.1** is the corresponding control table. Experimental module is shown in **Figure 4.2**.

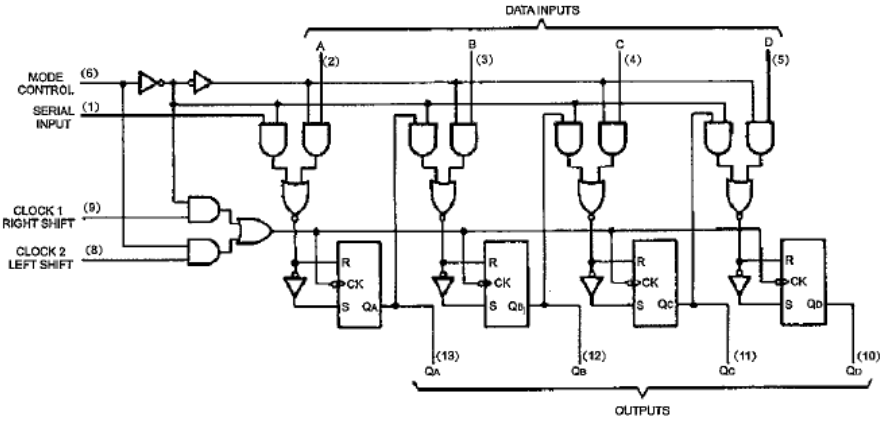
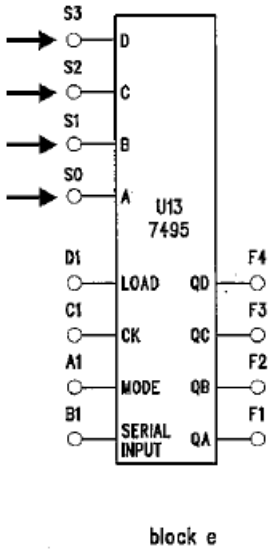


Figure 4.1

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2(L)	CLOCKS 1(R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_{B}↑	Q_{C}↑	Q_{D}↑	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

Table 4.1



block e

Figure 4.2

2. Connect A to SW0, B to SW1, C to SW2, D to SW3, F1 to L1, F2 to L2, F3 to L3, F4 to L4, D1 (Load) to the A of Pulse A, C1 (CK) to the B of Pulse B, B1 (IP) to SW7 and A1 (Mode) to SW6, as shown in **Table 4.2**.

INPUT			**Operation**
MODEL CONTROL	**C1**	**D1**	
L	⎍	X	Right Shift
H	X	⎍	Load Data

Table 4.2

3. Apply the input sequences in **Table 4.3** and record the results.

C1	B1	A1	F1	F2	F3	F4
⎍	**1**	**0**				
⎍	**1**	**0**				
⎍	**1**	**0**				
⎍	**1**	**0**				
⎍	**1**	**0**				
⎍	**0**	**0**				
⎍	**0**	**0**				
⎍	**0**	**0**				
⎍	**0**	**0**				
⎍	**0**	**0**				

Table 4.3

4. Set A1 and B1 to "1" (load). Apply the input sequences in **Table 4.4** and enter a positive pulse to D1. Record the results and discuss your observation.

INPUT					OUTPUT			
D1	**D**	**C**	**B**	**A**	**F1**	**F2**	**F3**	**F4**
⎍	0	0	1	0				
⎍	1	0	1	0				
⎍	1	1	1	0				
⎍	0	1	1	1				
⎍	0	1	1	0				

Table 4.4

Electronic Engineering Laboratory 1

SMJE 1062

LAB 5

SEQUENTIAL LOGIC CIRCUITS

Experiment 1: **Asynchronous Binary and Decade Up-Counter**

Experiment 2: **Synchronous Binary Up/Down Counter**

Experiment 3: **Presetable Binary Up/Down Counter**

Experiment 4: **Johnson Counter**

Experiment 1: Asynchronous Binary and Decade Up-Counter

OBJECTIVE

Understanding the principles of counters and how to construct counters with J-K flip-flops.

EQUIPMENTS REQUIRED

KL-32001 Advanced Digital Logic Lab ; Module KL-34004; Oscilloscope

PROCEDURES

(a) Asynchronous Binary Up-Counter

1. Follow the circuit scheme in **Figure 1.1** to construct the circuit of **Figure 1.2**.

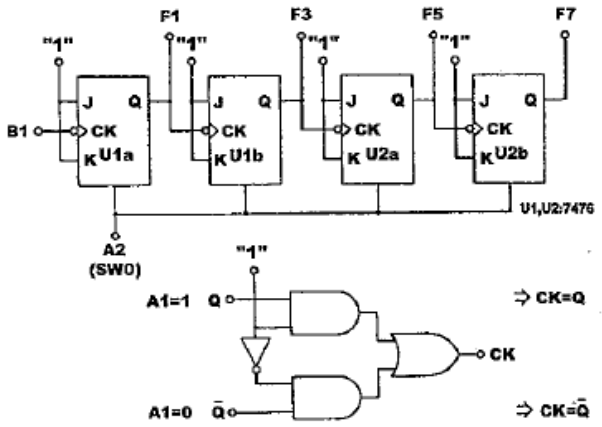


Figure 1.1

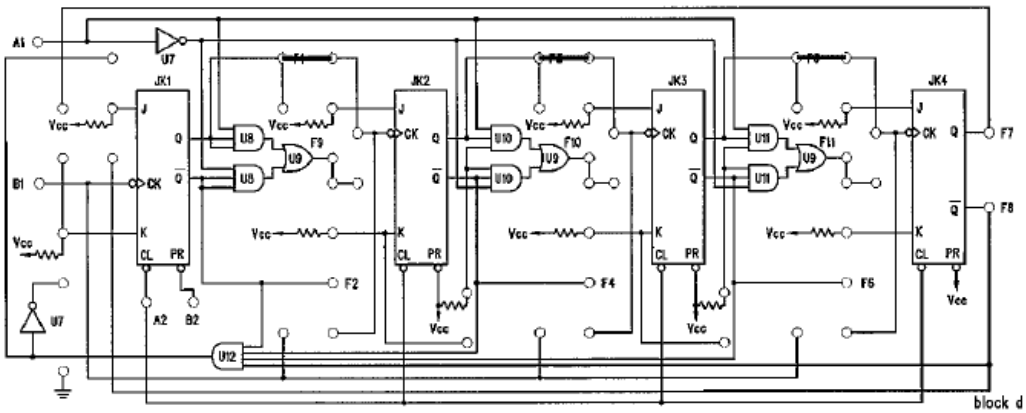


Figure 1.2

2. Connect A2(Clear) to SW0; A1 to SW1, B2(PR) to SW2, outputs F1, F3, F5, F7 to L1-L4 respectively and B1(CK) to the Clock Generator, adjust the output frequency to 1kHz.
3. Set A1 and B2 to HIGH, SW0 to LOW initially to clear the output; then set SW0 to HIGH to begin counting. Measure CK and the outputs with the oscilloscope, and record the outputs in **Figure 1.3**. **Figure 1.4** shows the reference waveforms.

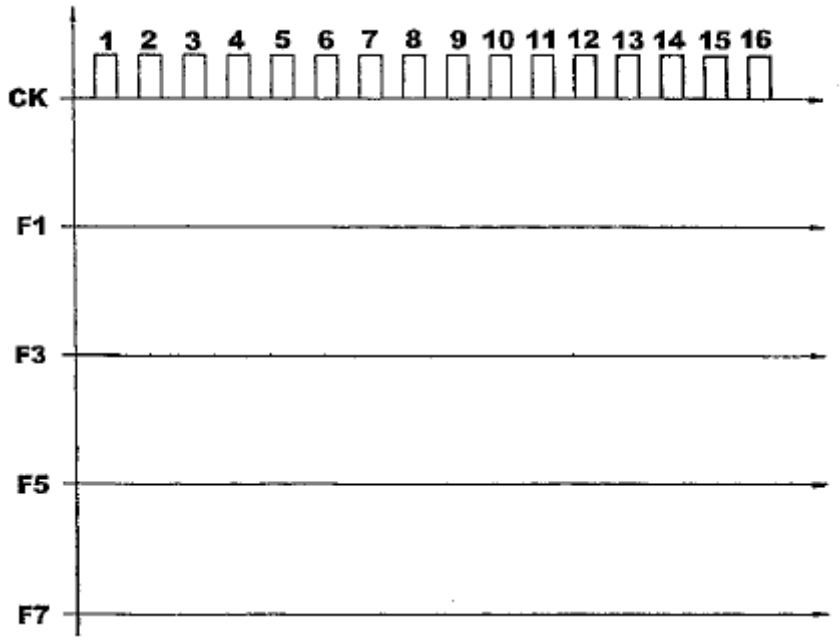


Figure 1.3

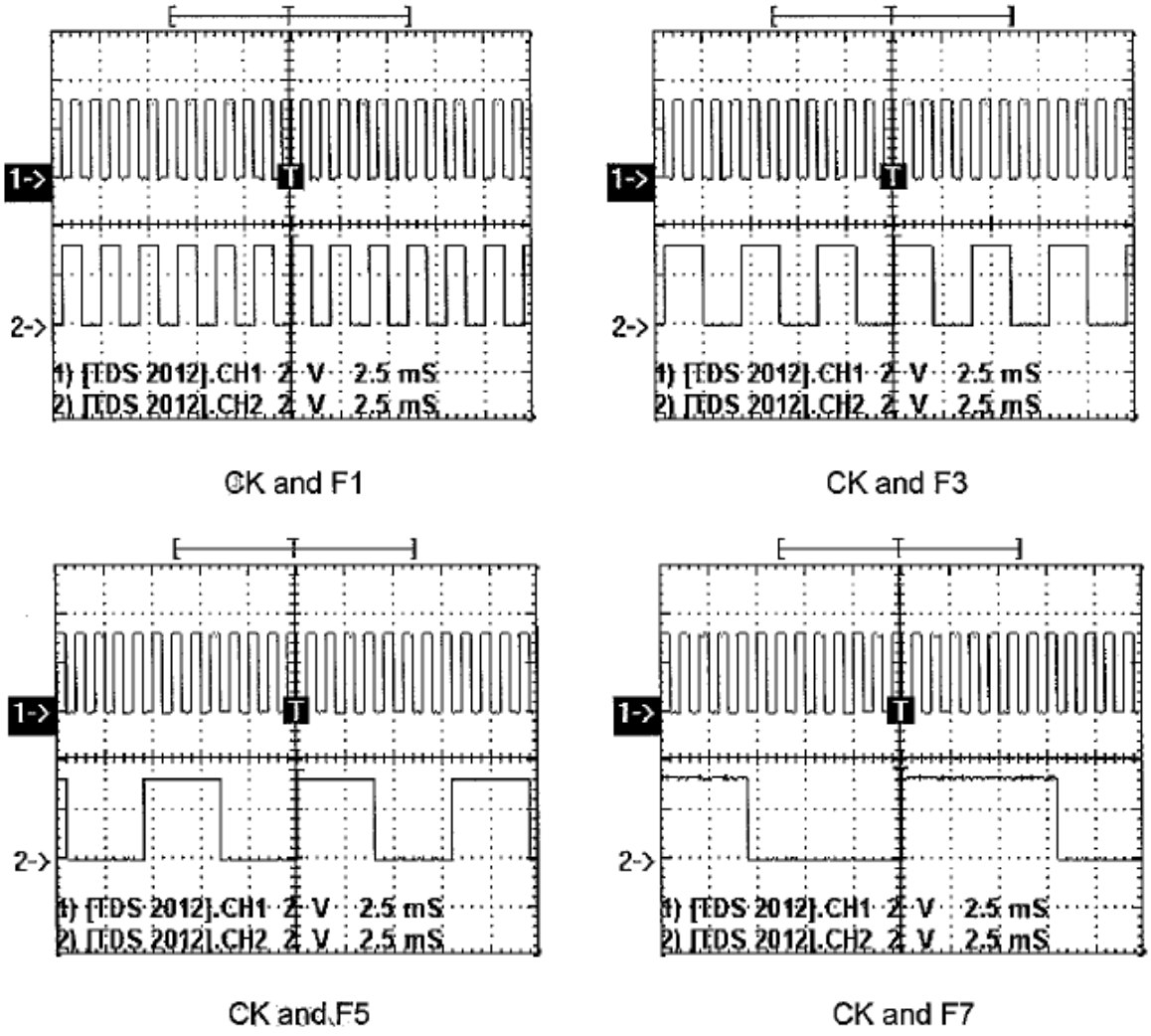
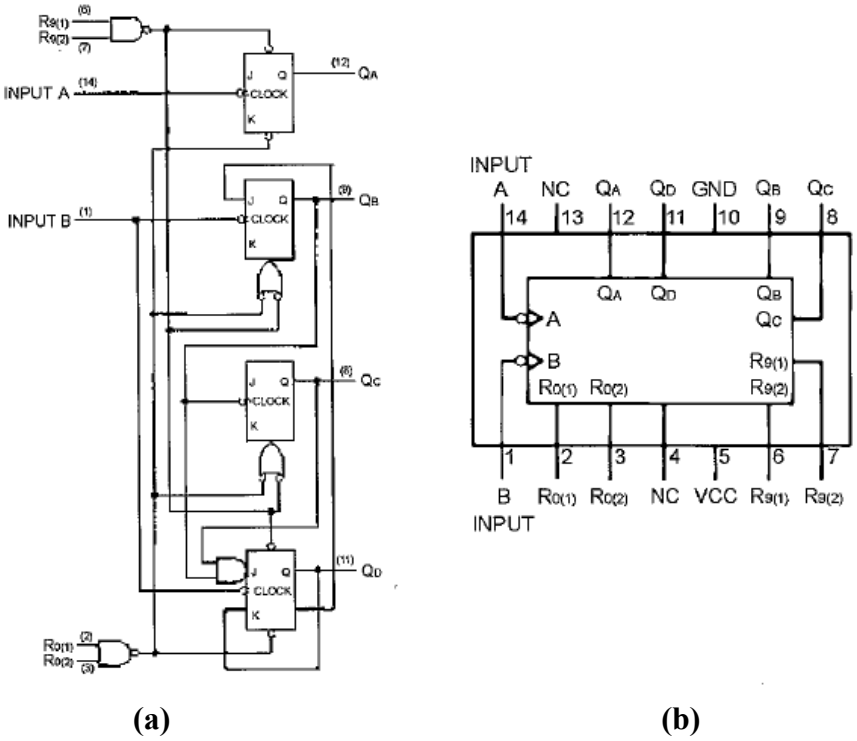


Figure 1.4

4. What happens if SW0 is set to LOW during the counting process? What are the maximum and minimum frequencies of the counter? Record them for discussion.
5. Enter the clock from 1kHz to 500kHz, and measure the waveforms of CK, F1, F3, F5 and F7 using oscilloscope and record the results for analysing and discussion.

(b) Asynchronous Decade Up-Counter

1. The 7490 IC contains four masterslave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-five. The inner structure is shown in **Figure 1.5 (a)** and the corresponding pin definition is shown in **Figure 1.5 (b)**. The experimental module KL-34004 is shown in **Figure 1.6**.



(a) **(b)**

Figure 1.5

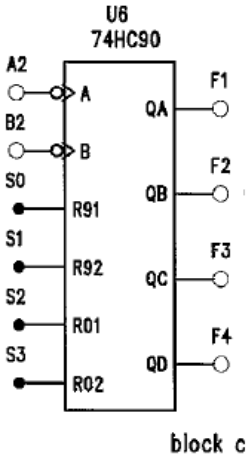


Figure 1.6

2. Connect S0-S3 of block e to SW0-SW3, F1-F4 to L1-L4; A2 to A of Pulse A, B2 to F1.
3. Connect S0, S1, S2 and S3 to ground and A2 to A of Pulse A. Measure and record the results in **Table 1.1**.

A2	QD	QC	QB	QA
⎍				
⎍				
⎍				
⎍				
⎍				
⎍				
⎍				
⎍				
⎍				
⎍				

Table 1.1

4. Connect F1 to B2; and enter 1 kHz pulse to A2. Measure and record A2(CK), F1, F2, F3, F4 in **Figure 1.7**.
5. Enter the clock from 1kHz to 500kHz. Measure the waveforms of CK, F1, F2, F3 and F4 using oscilloscope and record the results for analysing and discussion.

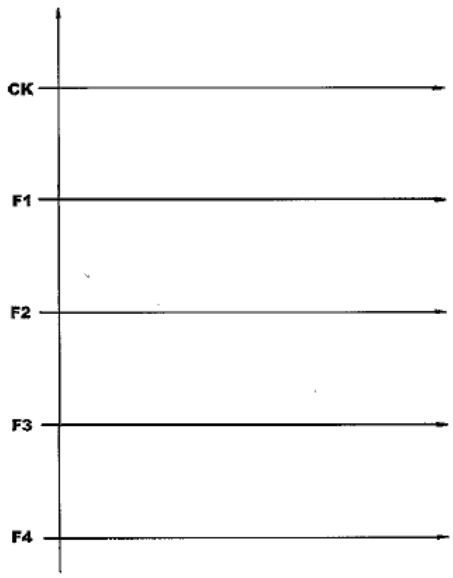


Figure 1.7

Experiment 2: Synchronous Binary Counter

OBJECTIVE
Understanding how to construct a synchronous binary counter

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34004; Oscilloscope

PROCEDURES

All procedures in this experiment refers to **block d** in the Module KL-34004.

(a) Synchronous Binary Up-Counter

1. The complete circuit of a binary up counter is shown in **Figure 2.1**. The corresponding truth table is shown in **Table 2.1**.

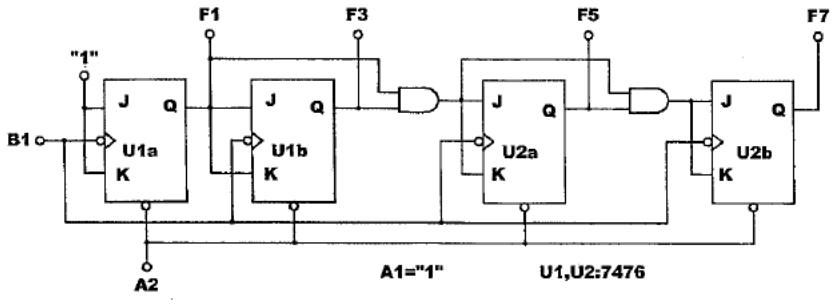


Figure 2.1

Counting number	CK	First-Digit QA	Second-digit QB	Third-digit QC	Fourth-digit QD
0	⎍	0	0	0	0
1	⎍	1	0	0	0
2	⎍	0	1	0	0
3	⎍	1	1	0	0
4	⎍	0	0	1	0
5	⎍	1	0	1	0
6	⎍	0	1	1	0
7	⎍	1	1	1	0
8	⎍	0	0	0	1
9	⎍	1	0	0	1
A	⎍	0	1	0	1
B	⎍	1	1	0	1
C	⎍	0	0	1	1
D	⎍	1	0	1	1
E	⎍	0	1	1	1
F	⎍	1	1	1	1

Table 2.1

2. An up counter scheme (the combination first stage's output Q with AND to enable JK of next stage) and a down counter scheme (the combination first stage's output $\bar{Q}$ with AND to enable JK of next stage) are combined as an up/down counter with AND-OR logic gates, as shown in **Figure 2.2**.

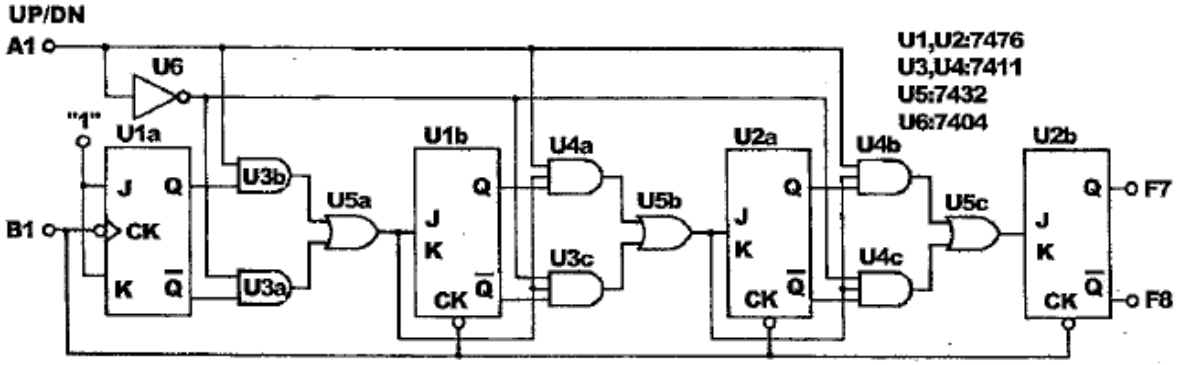


Figure 2.2

3. Construct a synchronous binary up counter as shown in **Figure 2.3**. Set A1 to HIGH.

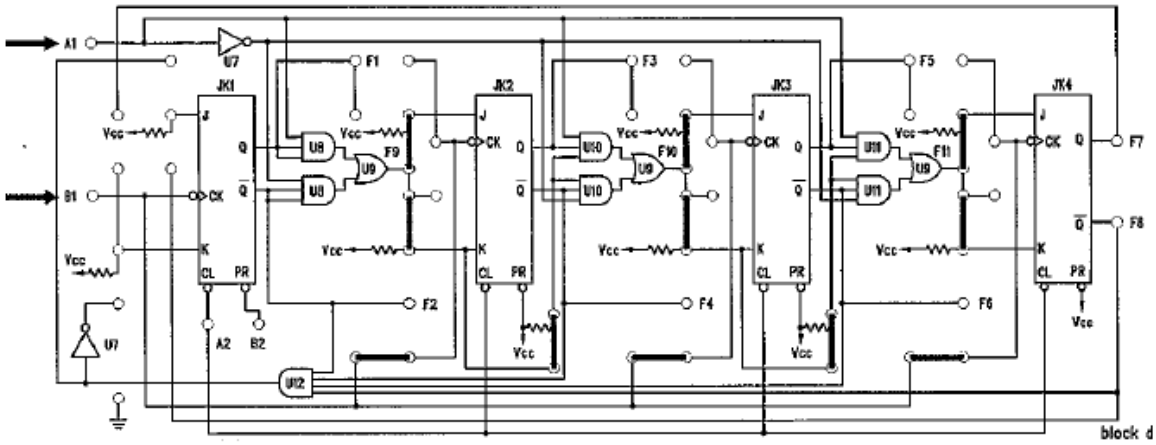


Figure 2.3

4. Connect A1 and A2 to SW0 and SW1 respectively, and set them to HIGH. Connect B1(CK) to the OUT of Clock Generator, and enter the clock from 10kHz to 100kHz. Connect B2 to SW2, and set it to HIGH. Using the 8-channel digital multiplexer on the unit panel, measure the waveforms of CK, F1, F3, F5 and F7 simultaneously and sketch the output waveforms in **Figure 2.4** for analysing and discussion.

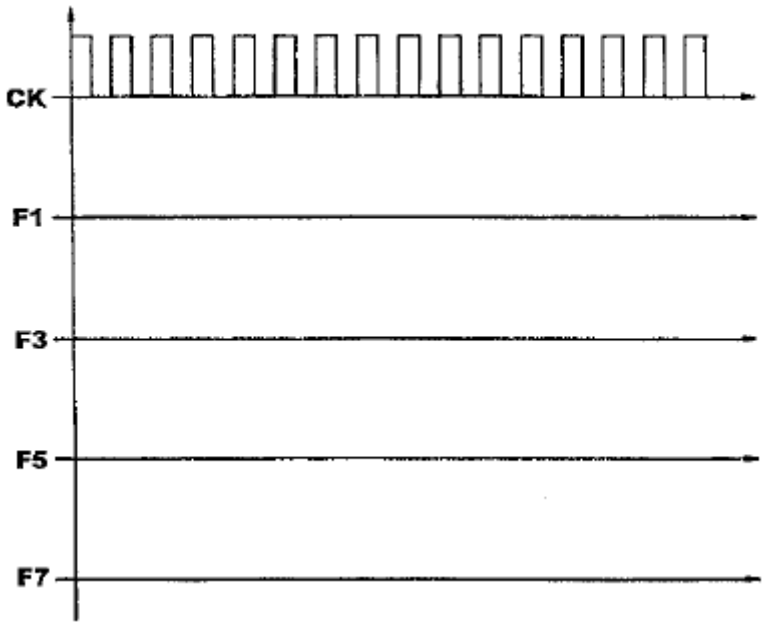


Figure 2.4

(b) Synchronous Binary Up/Down Counter

1. Construct a binary up/down counter circuit as shown in **Figure 2.3**. While A1=1, the circuit is set to up-counting. Contrarily, while A1=0, the counter is set to down-counting.
2. Connect A2 (Clear) to SW0; A1 to SW1; B2(PR) to SW2; outputs F1, F3, F5 and F7 to L1, L2, L3 and L4 respectively. Connect B1(CK) to the OUT of Clock Generator, and set it 1kHz. Set A1 and B2 to HIGH. Switch SW0 to HIGH. Measure the waveforms of CK, F1, F3, F5 and F7. **Figure 2.5** shows the reference waveforms.

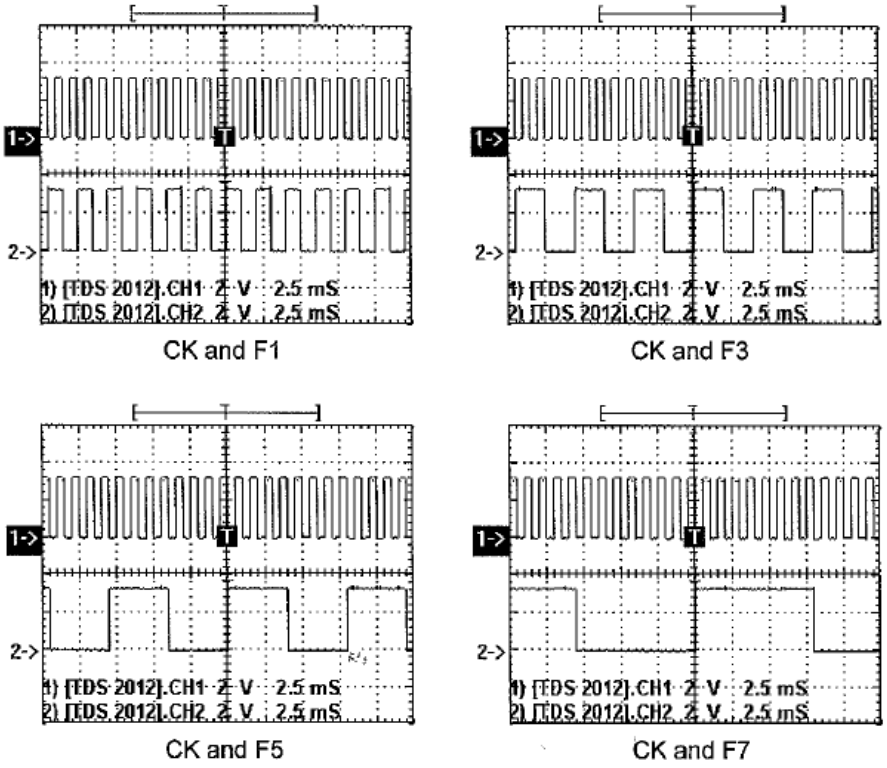


Figure 2.5

3. Set A1 to "0" and B2 to "1" for down counting. Measure the waveforms of CK, F1, F3, F5 and F7. **Figure 2.6** shows the reference waveforms.

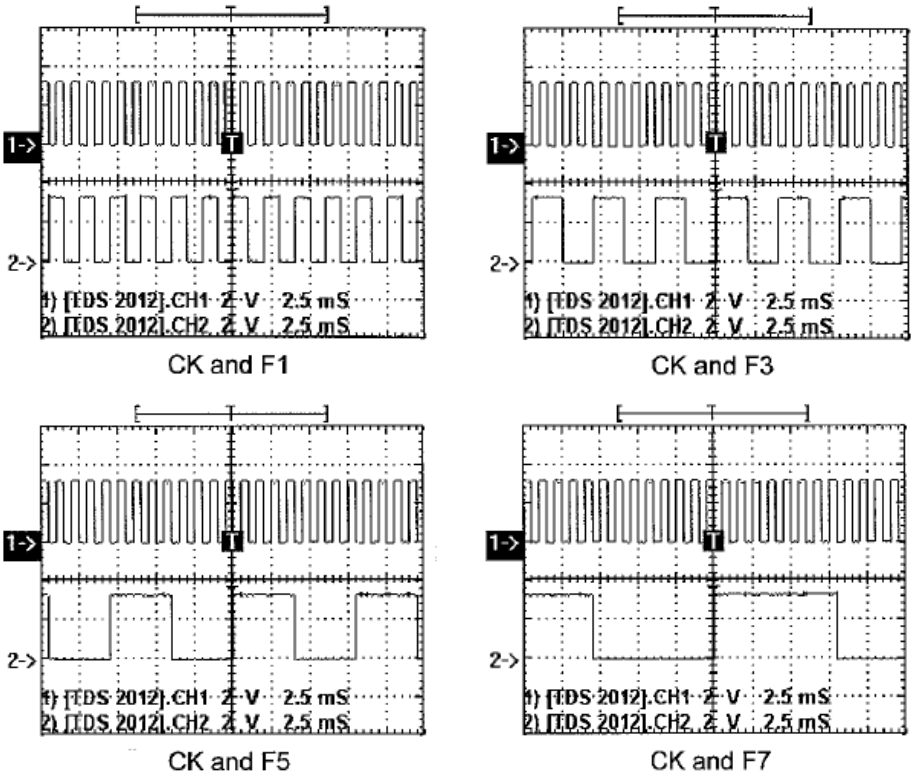


Figure 2.6

4. Enter the clock from 1kHz to 500kHz, and measure the waveforms of CK, F1, F3, F5 and F7 simultaneously and record the results in **Figure 2.7** for analysing and discussion.

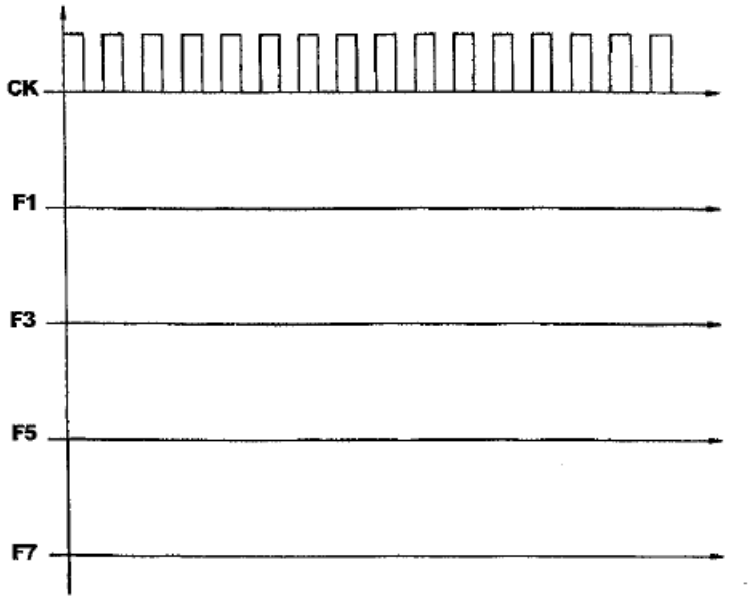


Figure 2.7

Experiment 3: Presetable Binary Up/Down Counter

OBJECTIVE
Understanding how to construct a presentable binary up/down counter

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34005; Oscilloscope

PROCEDURES

All procedures in this experiment refers to **block f** in the Module KL-34005.

1. As shown in **Figure 3.1**, set the pin "192/193" to SW7, and set it to LOW to make it running 74193 function. The truth table of 74193 is presented in **Table 3.1**.

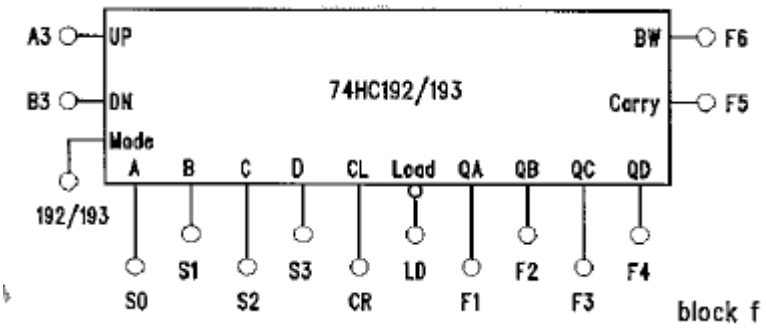


Figure 3.1

INPUT				OUTPUT			ACTIVE
CLEAR	$\overline{LOAD}$	COUNT UP	COUNT DOWN	QA QB QC QD	CARRY OUT	BORROW OUT	
L	H	↓	H	—	—	—	UP CONUT
L	H	H	↓	—	—	—	DOWN CONUT
L	↓ L	X	X	DA DB DC DD	—	—	DATA SET
↑ H	X	X	X	L L L L	—	—	CLEAR
X	X	↓ L	X	H H H H	↓ L	H	—
X	X	X	↓ L	L L L L	H	↓ L	—

Table 3.1

2. A3(UP) and B3(DN) are the inputs for up and down counting respectively. Pin "LD" is for data load (LOW enable) and connect it to SW5. Connect CR(Clear) to SW4, S0 to SW0, S1 to SW1, S2 to SW2 and S3 to SW3. Connect F1(QA) to L1, F2(QB) to L2, F3(QC) to L2, F3(QD) to L4, F5(carry) to L5 and F6(BW) to L6, and then connect F1-F4 to the decoding circuit "BCD-7Seg", and set the 7-segment display and INDEP mode (01).

(a) Up counting mode:

1. Set B3(DN) to SW6, and set it to HIGH. Set LD(Load) to HIGH and CR(CL) to LOW.
2. Input 1Hz to A3(UP), and set B3(DOWN) to HIGH (or set it to "HIGH"). Observe the 7-segment display and record the results in **Table 3.2**.

CK		**CK**		**CK**	
0		6		12	
1		7		13	
2		8		14	
3		9		15	
4		10			
5		11			

Table 3.2

(b) Load mode:

1. Connect CR to LOW and LD to LOW. Change the values of S0, S1, S2 and S3. The other conditions are not changed. Record the results of F4-F1 in **Table 3.3**.

INPUT				**OUTPUT**			
D	**C**	**B**	**A**	**F4**	**F3**	**F2**	**F1**
0	0	0	0				
0	0	1	0				
0	1	0	1				
0	1	1	1				
1	0	0	1				
1	0	0	0				
1	1	0	0				
1	1	0	1				
1	1	1	1				

Table 3.3

(c) Down counting mode:

1. Connect A3 to SW6 and set it to HIGH.
2. Connect F1 to L1, F2 to L2, F3 to L3, and F4 to L4. Connect F1-F4 to BCD-7Seg (7-segment display) of the unit, and set the 7-segment display at INDE mode (01). Connect LD(Load) to HIGH and CR(Clear) to LOW.
3. Input B3(DN) 1Hz clock, and record the status of 9-segment display in **Table 3.4**.

CK		**CK**		**CK**	
0		6		12	
1		7		13	
2		8		14	
3		9		15	
4		10			
5		11			

Table 3.4

Experiment 4: Johnson Counter

OBJECTIVE
Understanding how to construct a Johnson counter.

EQUIPMENTS REQUIRED
KL-32001 Advanced Digital Logic Lab ; Module KL-34004; Oscilloscope

PROCEDURES

All procedures in this experiment refers to **block d** in the Module KL-34004.

1. Construct a 4-bit Johnson counter by following the circuit scheme shown in **Figure 4.1**.

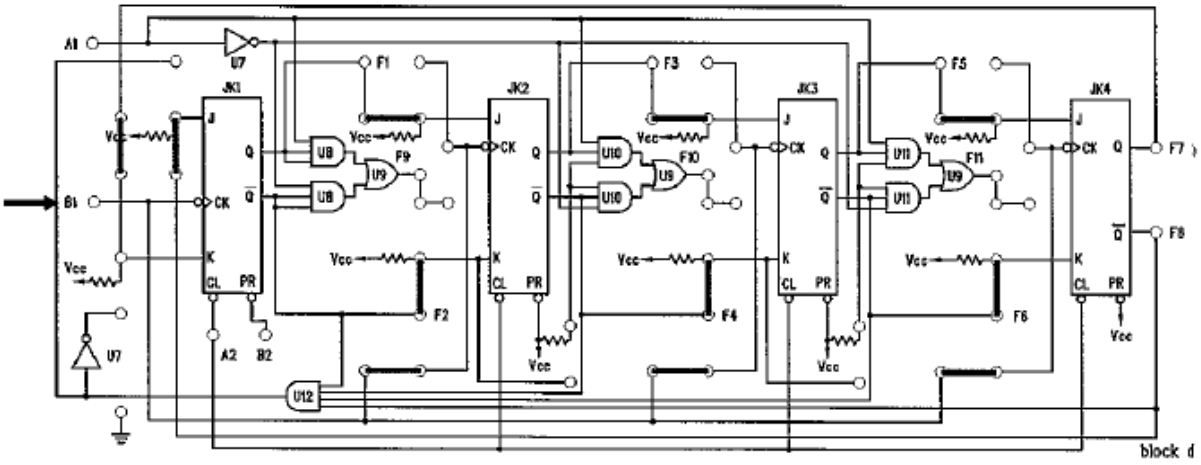


Figure 4.1

2. Connect A2 (Clear) to the $\bar{A}$ of Pulse A, B2 (Preset) to the $\bar{B}$ of Pulse B, B1(CK) to 1Hz of Standard Frequency. Connect outputs F1-F7 to L1-L7 respectively for LED display. Connect L1, L3, L5 and L7 to 7-segment display. Press Pulse A to set output "0000" and record the results in **Table 4.1**.
3. Enter the clock from 1kHz to 500kHz. Measure the waveforms of CK, F1, F3, F5 and F7 simultaneously and record the results in **Figure 4.3**.

CK	F7	F5	F3	F1
0				
1				
2				
3				
4				
5				
6				
7				
8				

Table 4.1

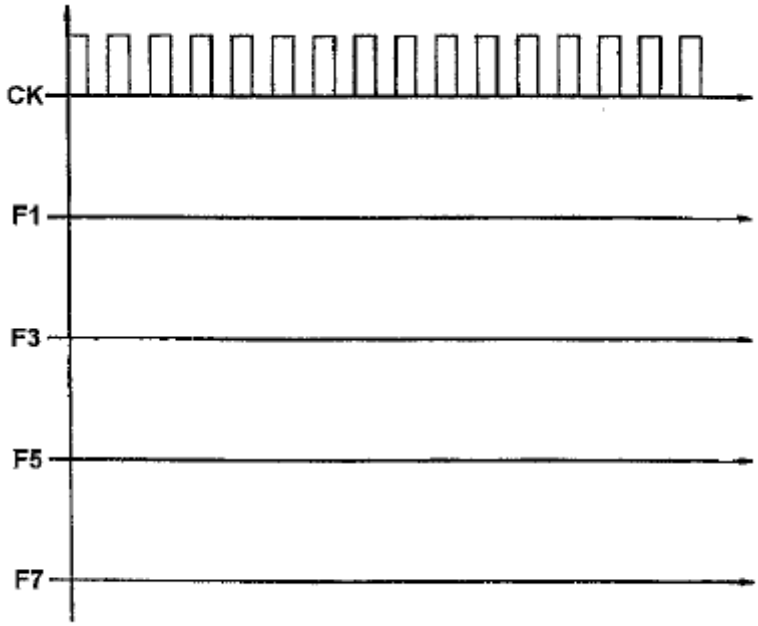


Figure 4.3