UTM UNIVERSITI TEKNOLOGI MALAYSIA

SEEE 1223
DIGITAL ELECTRONICS

CHAPTER 9:
PROGRAMMABLE LOGIC

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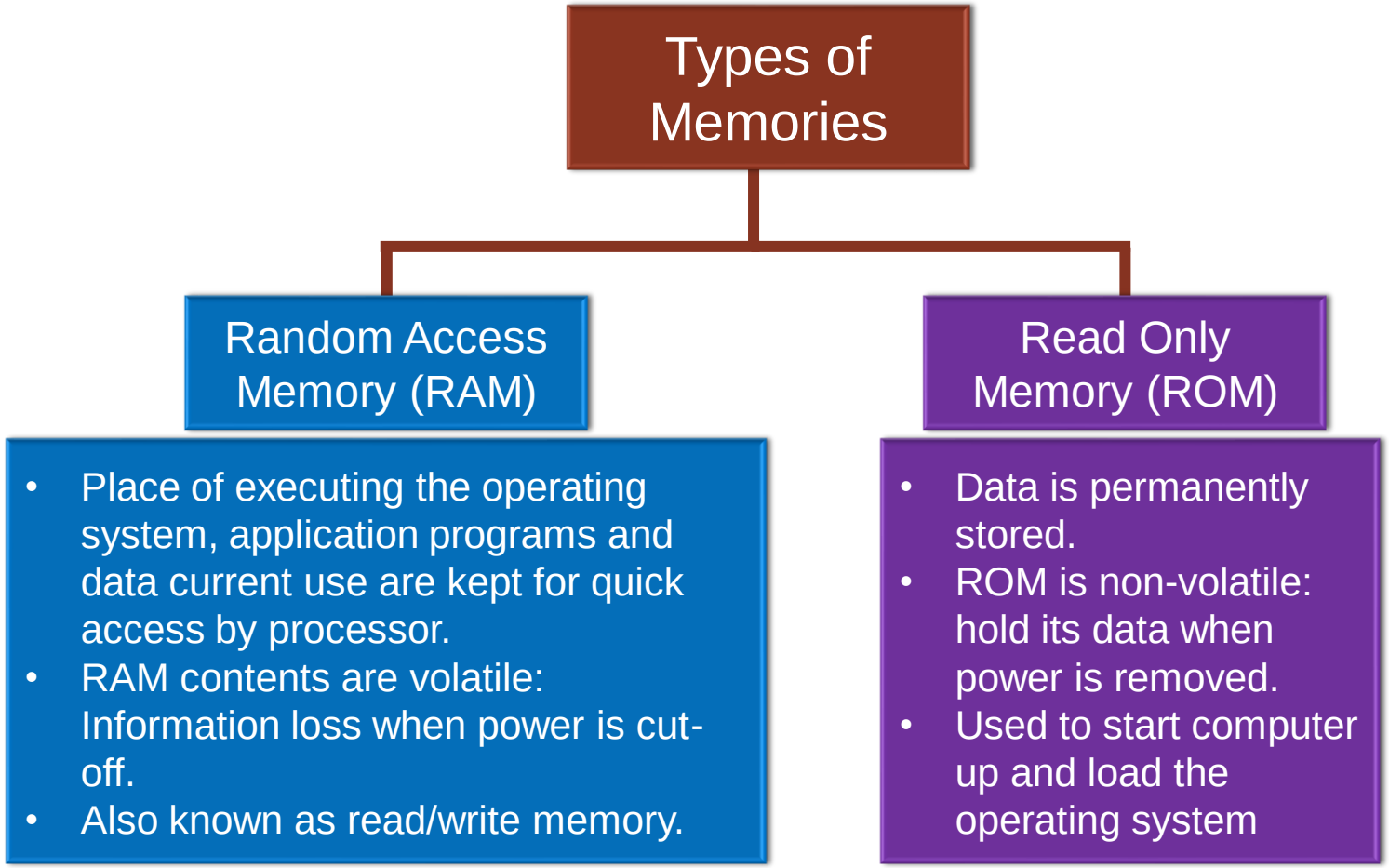
MEMORY: RAM & ROM

MEMORY
INTRODUCTION

- **Memories** are devices to which information is transferred for **storage** and from which information is available for **processing**.



MEMORY

RAM

- Integrated circuit RAM devices are available in two variations:
  1. **Static RAM (SRAM)**
     - Consist of internal latches that store the binary information.
     - Stored information remains valid as long as power is applied to the unit.
     - Faster.
     - High power consumption.
     - Expensive.
  2. **Dynamic RAM (DRAM)**
     - Stores binary information in the form of electric charges on capacitors provided by MOS transistors.
     - The charge of capacitors tend to decay with time, thus need to periodically recharge by refreshing the dynamic memory every few milliseconds.
     - Reduce power consumption.
     - Large number of memory words per chip.

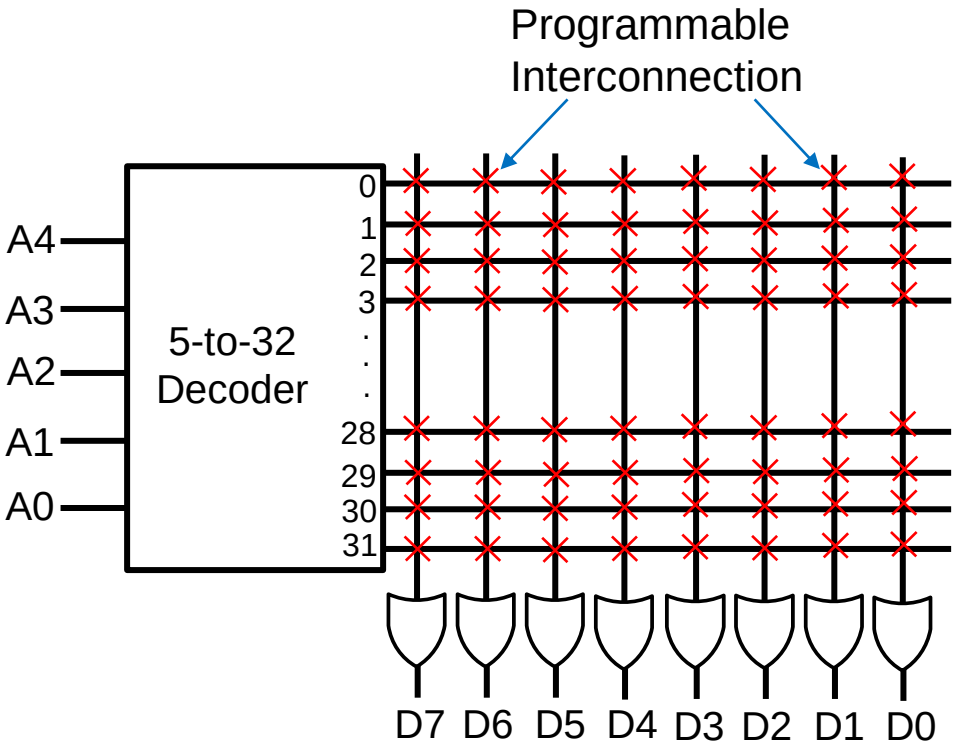
MEMORY

ROM

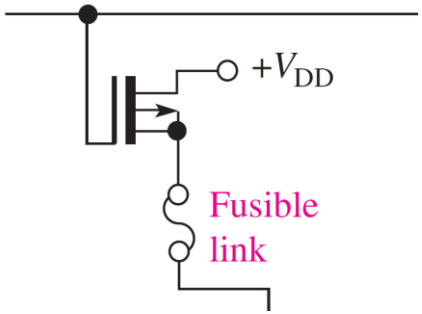
- Various types of ROM:
  1. **Mask Programmed ROM (MROM)**
     - Programmed using a mask during fabrication by manufacturer.
     - Advantages: high speed, high density, low unit costs.
     - Disadvantage: contents are permanent.
  2. **Programmable ROM (PROM)**
     - Contents are in the form fuses which are blown during programming.
     - Once blown, the fuses cannot be restored.
     - PROM is one time programmable (OTP): cannot be updated and reused after initial programming.

MEMORY

ROM



An unprogrammed 32 x 8 PROM



MEMORY

ROM

- Various types of ROM (cont.):
  3. **Erasable Programmable ROM (EPROM)**
     - Can be erased and reprogrammed many times.
     - The whole chip is erased by exposure to approximately 20 minutes of intense UV light.
  4. **Electrically-Erasable Programmable ROM (EEPROM)**
     - Can be erased and reprogrammed without requiring special burning equipment.
     - High costs.
     - Allows only one memory word to be written or erased at any one time.
  5. **Flash Memory**
     - High speed and high density.
     - Erases many locations simultaneously.
     - Can only tolerate about 10000 erase operations before the device fails.

MEMORY

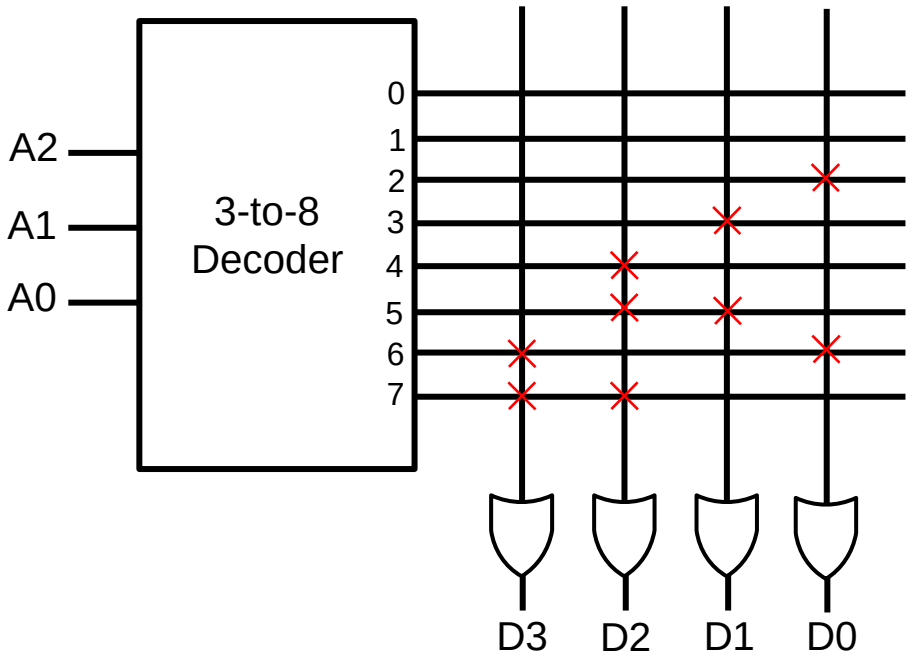
ROM

Example

Given the truth table of 8 x 4 ROM as follows. Find the number of programmable interconnections & implements the ROM circuit.

A2	A1	A0	D3	D2	D1	D0
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

Number of programmable interconnection:
$= 8 \times 4 = \mathbf{32}$



PROGRAMMABLE LOGIC DEVICE: PLA & PAL

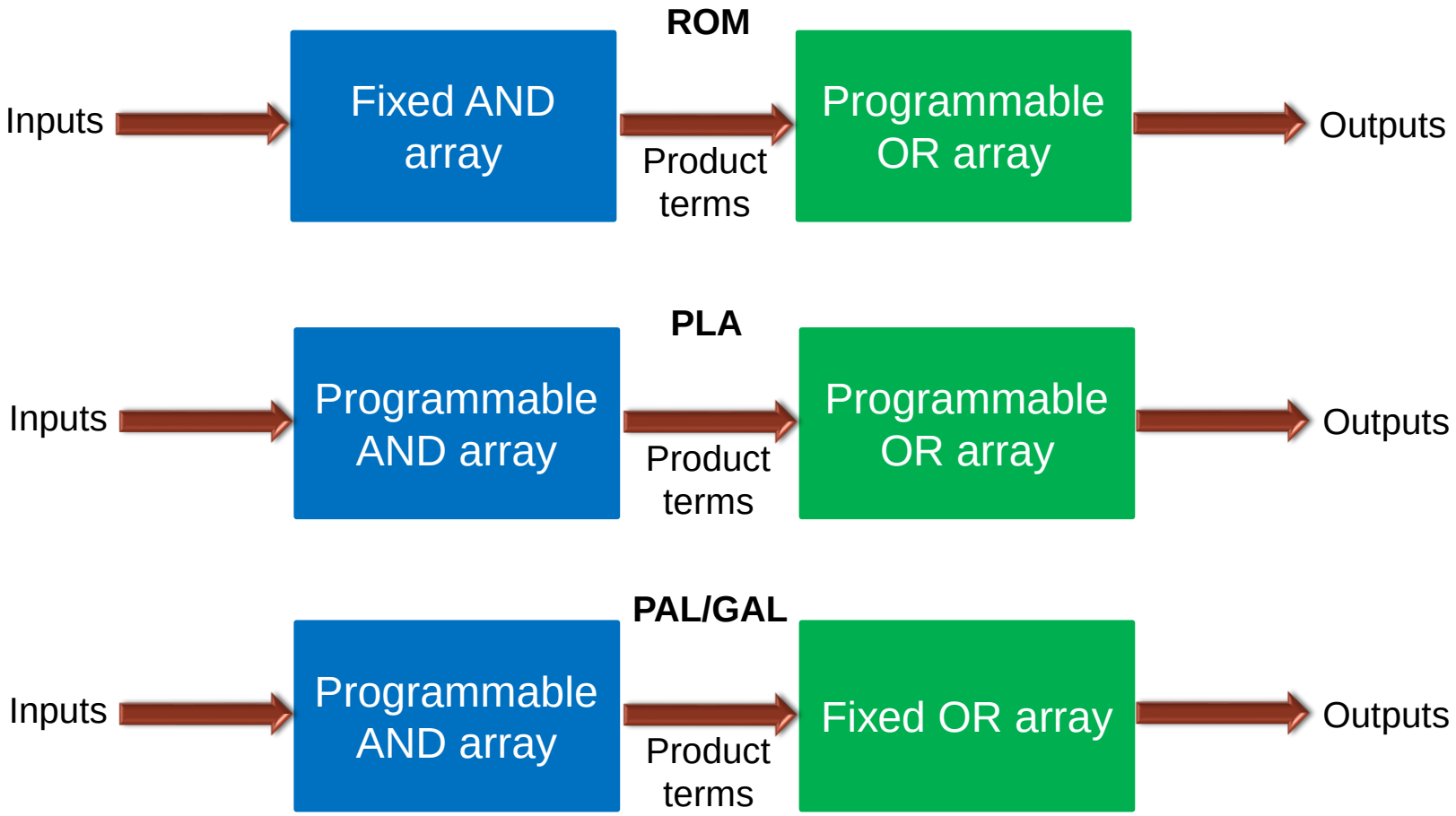
PROGRAMMABLE LOGIC DEVICE (PLD)

INTRODUCTION

- **PLD** consists of general purpose logic resources that can be connected according to the engineer's design.
- It must be programmed first before be used in circuit.
- **Advantages:** Fewer parts needed, reduce inventory cost, number of interconnections are decreases as more logic integrated into each chip, higher reliability.
- **Disadvantages:** Longer propagation delay, high power consumption.
- Example of PLD are:
  - **ROM**
  - **PLA**
  - **PAL**
  - **GAL**

PROGRAMMABLE LOGIC DEVICE (PLD)

INTRODUCTION



Three configurations of SPLDs

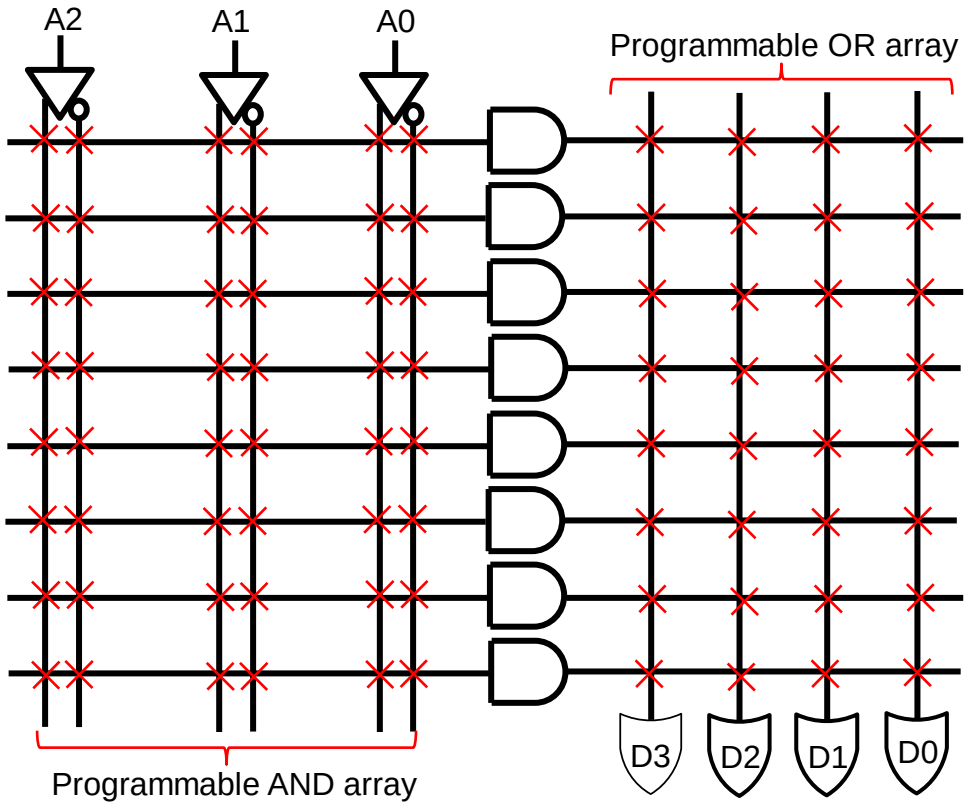
PROGRAMMABLE LOGIC DEVICE (PLD)

PLA

- **Programmable Logic Array (PLA)** consists of programmable AND and OR arrays.
  - ❖ **Advantageous when**
    - Relatively few unique minterm combinations.
    - Many minterms are shared among the output functions.
  - ❖ **Drawbacks**
    - Expensive to manufacture.
    - Poor speed performance: Thus PAL (Programmable Array Logic) and GAL (Generic Array Logic) were introduced.

PROGRAMMABLE LOGIC DEVICE (PLD)

PLA



× Programmable Interconnection

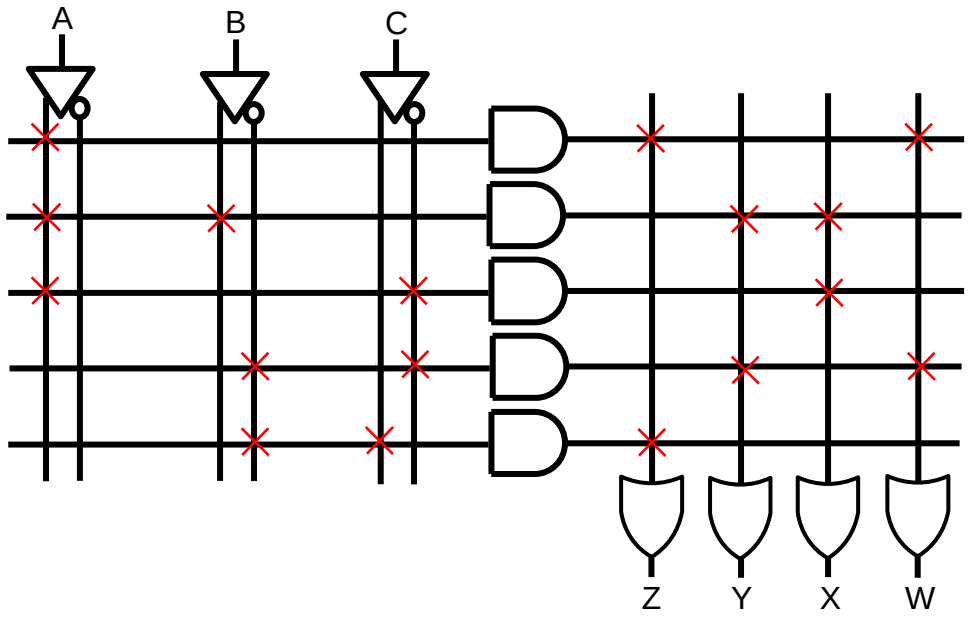
PROGRAMMABLE LOGIC DEVICE (PLD)

PLA

Example

Implement the following logic function using PLA.

$$W = A + \bar{B}\bar{C}$$
$$X = A\bar{C} + AB$$
$$Y = \bar{B}\bar{C} + AB$$
$$Z = \bar{B}\bar{C} + A$$



PROGRAMMABLE LOGIC DEVICE (PLD)

PAL

- **Programmable Array Logic (PAL)** provides an array of programmable AND gates, but the OR connections are fixed.
- Unlike PLA, product term cannot be shared among gates.
  - ❖ **Advantageous when**
    - Cheaper and faster.

GAL

- **Generic Array Logic (GAL)** has the same basic structure as PAL (Programmable AND Gates, OR connections are fixed), but being EEPROM-based: Can be erased and reprogrammed.
  - ❖ **GAL improves upon PAL in three aspects.**
    - Can be erased.
    - Can be programmed while installed in circuit.
    - Has programmable output stage or marcocells that has feedback to enable product term to be expanded and complementary output.

PROGRAMMABLE LOGIC DEVICE (PLD)

PAL/GAL