INSTRUCTIONS:

Answer all questions from Part A and B in this question booklet. For Part B, read the questions carefully and show ALL your works in details.

This examination will contribute 35% towards the total marks of 100 points.

Warning!
Students who are caught cheating during the examination will be reported to disciplinary board for action to suspend the student for one or two semesters.

(Please Write Your Lecturer Name And Section In Your Answer Booklet)

| Name       |                         |
| I/C No.    |                         |
| Year / Course |                     |
| Section   |                         |
| Lecturer Name |                   |

This question paper consists of ____ (__) printed pages excluding this page.
PART A: 15 OBJECTIVE QUESTIONS [Total mark 15 points]

Answer all the questions. Read each statement carefully. Please answer in Attachment A (page 10).

1. One of the parallel adder types that is based on how it handles a carry value is a _____ carry adder.
   A) generation
   B) look back
   C) override
   D) ripple

2. A decoder uses _________ gate if we want the output to be HIGH.
   A) AND
   B) OR
   C) NAND
   D) XNOR

3. Choose the FALSE statement about DEMUX.
   A) It is also known as a data selector.
   B) A DEMUX is basically the reverse of the multiplexing function.
   C) It takes digital information from one line and distributes it to a given number of output lines.
   D) A decoder can also be used as a DEMUX.

4. Select the CORRECT characteristic of the Figure 1 above.
   A) It is a negative edge-triggered flip-flop.
   B) It is a negative edge-triggered latch.
   C) It is a positive edge-triggered flip-flop.
   D) It is a positive edge-triggered latch.

Figure 1
5. Which of the following statements is FALSE about the characteristics of sequential and combinational logic circuits?
   A) Combinational logic circuit does not contain memory element compared to sequential logic circuit.
   B) In order to be fully functional, both combinational and sequential logic circuits require input clock triggered.
   C) Sequential logic circuit considers the previous state output before the current output circuit is produced.
   D) Sequential logic circuit can be constructed using basic logic gates and memory devices.

6. Which of the following statements is FALSE about a latch and a flip-flop?
   A) Latch and flip-flop can store binary bit 0 or 1.
   B) A latch requires a clock input before output latch can be changed.
   C) A flip-flop output will change according to the input flip-flop at edge triggered.
   D) A latch output will change according to the input level of the latch.

7. Which of the following statements is FALSE about an S-R latch?
   A) It has a SET state.
   B) It has a RESET state.
   C) It has a HOLD state.
   D) It has a TOGGLE state.

8. How many different states does a 3-bit asynchronous counter has?
   A) 3
   B) 6
   C) 8
   D) 9

9. What is the state value (in decimal) of Q2, Q1 and Q0 in the following circuit in order to produce a HIGH output at X?

   ![Circuit Diagram]

   A) 5
   B) 6
   C) 7
   D) 8
10. What is the maximum state of a typical MOD 10 (decade) binary counter?
   A) 0000  C) 1111
   B) 1010  D) 1001

11. [Figure 2]

   Referring to Figure 2, what is the signal frequencies of X and Y?
   A) X = 0.25 MHz, Y = 0.125 MHz.
   B) X = 4 MHz, Y = 2 MHz.
   C) X = 0.125 MHz, Y = 0.25 MHz.
   D) X = 2 MHz, Y = 4 MHz.

12. Which of the following statements is **TRUE** about synchronous counter?
   A) Synchronous counter can count up and count down simultaneously (with the same clock cycle).
   B) If synchronous counter is implemented with N flip-flops in its sequential circuit, the number of valid states of the counter is always $2^N$.
   C) **Synchronous counter can be implemented using D flip-flops, as long as the clock source of the flip flops is taken from the common clock source.**
   D) Synchronous counter can be implemented using any type of flip-flop, as long as the clock source of flip-flops is taken from the output of the preceding flip-flops.

13. The following are Shift Registers, **EXCEPT**:  
   A) SISO Serial In, Serial Out  C) SILO Serial In, Last Out  
   B) SIPO Serial In, Parallel Out  D) PIPO Parallel In, Parallel Out

14. The following statements are true about Shift Register (SR) **EXCEPT**:
   A) SR stores binary data  C) SR consists of several latches  
   B) SR performs data rotate  D) SR is used for data transfer

15. A **MOD 10** Ring counter requires __________.
   A) ten flip-flops  C) four flip-flops  
   B) five flip-flops  D) eight flip-flops
PART B: 4 SUBJECTIVE QUESTIONS [Total mark 85 points]

Question 1 [15 Marks]
Answer the following questions about some functions of combinational logic.

(a) A logic symbol of a parallel adder for summing TWO binary numbers is illustrated in Figure 3. If \( A = 0011_2 \) and \( B = 0110_2 \) with the carry in, \( C_0 = 0 \), complete Table 1 by reproducing it in your answer booklet. Assume pin label 1 represents LSB. [4M]

![Figure 3](image)

<table>
<thead>
<tr>
<th>Pin Label (i)</th>
<th>Input</th>
<th>Carry Out</th>
<th>Sum</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( A_i )</td>
<td>( B_i )</td>
<td>( C_i )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

(b) Draw the logic circuit for a binary decoder to detect the binary code 10010 which produces an active-LOW output. Assume the inputs are represented as \( A_4A_3A_2A_1A_0 \). [3M]

Answer:

![Logic Circuit](image)
(c) Given an active HIGH 7-segment display in Figure 4 displaying a digital number from a decoder that based on the BCD value, fill in Table 2. Reproduce Table 2 in your answer booklet.

![Figure 4](image)

<table>
<thead>
<tr>
<th>BCD Input</th>
<th>Segment Output</th>
<th>Display</th>
</tr>
</thead>
<tbody>
<tr>
<td>A B C D</td>
<td>a b c d e f g</td>
<td></td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>0 1 1 0 1 0 0</td>
<td>4</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>1 1 1 0 0 0 0</td>
<td>7</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>1 1 1 1 0 1 1</td>
<td>9</td>
</tr>
</tbody>
</table>

(d) Figure 5 (in page 11) shows the waveforms of data-input $D_i$ and data-select $S_i$ applied to a multiplexer. Complete Figure 5 by drawing the waveform output of $X$ in relation to the inputs. Label each segment of output $X$ with the correct data input selection.

![Figure 5](image)

**Question 2 [15 Marks]**

(a) Figure 6 shows a basic circuit of a latch. Answer the following based on the circuit.

![Figure 6](image)
(i) Complete the following truth table with initial values of $Q$ and $\overline{Q}$ are bit 1 and 0.

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[
\begin{array}{ccc}
\text{A} & \text{B} & \text{Q} & \overline{\text{Q}} & \text{State} \\
0 & 0 & \text{NC} & \text{NC} & \text{No change} \\
0 & 1 & 0 & 1 & \text{Latch RESET} \\
1 & 0 & 1 & 0 & \text{Latch SET} \\
1 & 1 & 0 & 0 & \text{Invalid} \\
\end{array}
\]

(ii) What type of latch is represented by the circuit in Figure 6? [1M]

SR Latch, Active High SR Latch

(b) Referring to Figure 7 in page 12, complete the output $Q$ for a Gated $\overline{S}$ - $\overline{R}$ latch. Label each state that occurs for each transition in the timing diagram. [3M]

(c) Referring to Figure 8, answer the following questions. Assume $Q$ is initially low.

(i) Draw output $\overline{Q}$ in the timing diagram at page 12. [3M]

(ii) List the input priority of the flip-flop from the highest to the lowest. [2M]

PRE, CLR
CLK
JK

(d) Draw the implementation of negative edge T flip-flop by using JK flip-flop. [2M]
Question 3 [40 Marks]

(a) Based on Figure 9, draw the State Diagram for the counter by using binary representation. [4M]
(b) Redesign Figure 9, by considering new requirements as follows:

- 3-bit count up ripple counter with Modulus-5;
- using J-K Flip-Flop and
- with negative edge triggered clock.

(c) Rolek Corp is designing its new 2-bit binary counter. The state diagram of the counter is given in Figure 10:

![State Diagram for 2-bit Rolek binary synchronous counter](image)

**Figure 10: State Diagram for 2-bit Rolek binary synchronous counter**

Using T flip-flops, design the sequential logic circuit of the latest Rolek binary counter as
specified above, by answering all questions below.

(i) Complete the following Next State and Transition Table. [8M]

<table>
<thead>
<tr>
<th>Input</th>
<th>Present State</th>
<th>Next State</th>
<th>FF₁</th>
<th>FF₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>m</td>
<td>Q₁</td>
<td>Q₀</td>
<td>T₁</td>
<td>T₀</td>
</tr>
</tbody>
</table>

(ii) Get the optimized SOP Boolean expressions using K-Map. [4M]

\[
T₁ = m'Q₀Q₁ + mQ₀Q₁'
\]

\[
T₀ = m'Q₁'Q₀ + mQ₀Q₁'
\]
(iii) Draw the complete final circuit design. [3M]

(d) For the sequential circuit shown in Figure 11, answer the following questions:

Figure 11: Sequential Circuit
(i) Derive the next-state equations for each flip-flop and output Y. [3M]

\[ Q_{1+} = D_1 = Cnt \ XOR \ Q_1 \]
\[ Q_{0+} = D_0 = (Q_0') \]
\[ Y = Q_0 + Q_1 \]

(ii) Produce the next state table. [8M]

<table>
<thead>
<tr>
<th>Input, Cnt</th>
<th>Present State</th>
<th>Next State</th>
<th>Output, Y</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Q1</td>
<td>Q0</td>
<td>Q1_+ = D1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
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<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

(iii) Draw the state diagram. [4M]
Question 4 [15 Marks]

(a) Initially at \( t_0 \), a 5-bit SIPO shift register is cleared. Then, at \( t_1 \) the data word 19\(_{10}\) is serially entered. LSB is shifted in first.

(i) Draw the circuit for a 5-bit SIPO using D flip-flop. \[3M\]

(ii) What are the content of the SIPO shift register at \( t_3 \)? Show your works in a table form. \[3M\]

<table>
<thead>
<tr>
<th>Data</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>FF1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>FF2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>FF3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>FF4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

(iii) At what clock cycle can all the input data be read at the output and state the output \[2M\]

After 5 clock cycle data can be read at the output.

Output:

| Data | 1 | 0 | 0 | 1 | 1 |
(b) Answer the following questions based on a Johnson counter.

(i) Draw the logic diagram for a MOD 8 Johnson counter. [3M]

(ii) Write the counting sequence in a table form. Initially the content of all flip-flops are binary ‘0’. [4M]

<table>
<thead>
<tr>
<th>Clock, t</th>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
<th>Q0</th>
<th>Q0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
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<tr>
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<tr>
<td>3</td>
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<tr>
<td>4</td>
<td>1</td>
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</tr>
<tr>
<td>5</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
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<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
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</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

All the best!!! Show ALL your works.
ATTACHMENT A

<table>
<thead>
<tr>
<th>Name</th>
<th>Matric No.</th>
<th>Lecturer</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Dr. Foad</td>
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<td>Ms Rashidah</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ms. Marina</td>
</tr>
</tbody>
</table>

PART A (OBJECTIVE)

Mark your answer clearly.

Example: =A= =B= =C= =D=

1. =A= =B= =C= =D=
2. =A= =B= =C= =D=
3. =A= =B= =C= =D=
4. =A= =B= =C= =D=
5. =A= =B= =C= =D=
6. =A= =B= =C= =D=
7. =A= =B= =C= =D=
8. =A= =B= =C= =D=
9. =A= =B= =C= =D=
10. =A= =B= =C= =D=
11. =A= =B= =C= =D=
12. =A= =B= =C= =D=
13. =A= =B= =C= =D=
14. =A= =B= =C= =D=
15. =A= =B= =C= =D=

Objectives /15
Question 1 /15
Question 2 /15
Question 3 /40
Question 4 /15
Total /100

14
Answer for Question 1 (d)

Figure 5

(Data In (D_i))

Answer:

X
Answer for Question 2 (b)

Figure 7
Answer Question 2 (c)(i)