Scoreboard Dynamic Scheduling

Four Stages of Scoreboard Control: ISSUE

1. Issue: decode instructions & check for structural hazards (ID1)

   If a functional unit for the instruction is free and no other active instruction has the same destination register (WAW), the scoreboard issues the instruction to the functional unit and updates its internal data structure. If a structural or WAW hazard exists, then the instruction issue stalls, and no further instructions will issue until these hazards are cleared.

Algorithm:

- Assure In-Order issue
- Multiple issues per cycle are allowed
- Check if Destination Register is already reserved for writing (WAW)
- Check if Read-Operand stage of Functional Unit is free (Structural)

Four Stages of Scoreboard Control: READ-OPERANDS

2. Read operands: wait until no data hazards, then read operands (ID2) – First Functional Pipeline Stage

A source operand is available if no earlier issued active instruction is going to write it, or if the register containing the operand is being written by a currently active functional unit. When the source operands are available, the scoreboard tells the functional unit to proceed to read the operands from the registers and begin execution. The scoreboard resolves RAW hazards dynamically in this step, and

Algorithm:

- ☐ Wait for operands to become available, Register Result Status (RAW)
- ☐ Operand Caching is allowed
- ☐ Forwarding from another WB stage is allowed

Four Stages of Scoreboard Control – ex + write

3. Execution: operate on operands (EX)
   - The functional unit begins execution upon receiving operands. When the result is ready, it notifies the scoreboard that it has completed execution. This stage can be (sub-)pipelined.
4. Write result: finish execution (WB)
   - Once the scoreboard is aware that the functional unit has completed execution, the scoreboard checks for WAR hazards.
     If none, it writes results. If WAR, it stalls the instruction.

Algorithm:

- Delay write until all Rj and Rk fields for this register are marked as either cached or read.
  - If caching of operands is done: forward answer right away.
  - If not, wait until all operands are read before writing.
- Forward answers to units waiting for this write for their operand.

Three Parts of the Scoreboard

1. Instruction status
   - Indicates which of 4 steps the instruction is in.
2. Functional unit status
   - Indicates the state of the functional unit (FU). 9 fields for each functional unit
     - Busy – Indicates whether the unit is busy or not
     - Op – Operation to perform in the unit (e.g., + or -)
     - Fi – Destination register
     - Fj, Fk – Source-register numbers
     - Qj, Qk – Functional units producing source registers Fj, Fk
     - Rj, Rk – Flags indicating when Fj, Fk are available and not yet read. (Alternatively: read and cached)
3. Register result status:
   - Indicates which functional unit will write each register, if one exists. Blank when no pending instructions will write that register.

Scoreboard Example Cycle 1

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1			
LD	F2	45	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Clock 1

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F6		R2				Yes
Mult1	No								
Mult2	No								
Add	No								
Divide	No								

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU				Int					

R2 has not been read/cached until cycle 2!!!

Scoreboard Example Cycle 2

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2		
LD	F2	45	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Clock 2

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F6		R2				Yes
Mult1	No								
Mult2	No								
Add	No								
Divide	No								

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU				Int					

Issue 2nd LD or MULT?

Scoreboard Example Cycle 4

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3				
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Clock 4

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F6		R2				Yes
Mult1	No								
Mult2	No								
Add	No								
Divide	No								

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU				Int					

Scoreboard Example Cycle 5

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5			
MULTD	F0	F2	F4				
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Clock 5

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F2		R3				Yes
Mult1	No								
Mult2	No								
Add	No								
Divide	No								

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU		Int							

SUPERSCALAR: Issue MULTD?

Scoreboard Example Cycle 6

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6		
MULTD	F0	F2	F4	6			
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Clock 6

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F2		R3				Yes
Mult1	Yes	Mult	F0	F2	F4	Int		No	Yes
Mult2	No								
Add	No								
Divide	No								

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1	Int							

Scoreboard Example Cycle 7

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	
MULTD	F0	F2	F4	6			
SUBD	F8	F6	F2	7			
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Clock 7

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F2		R3				No
Mult1	Yes	Mult	F0	F2	F4	Int		No	Yes
Mult2	No								
Add	Yes	Sub	F8	F6	F2		Int	Yes	No
Divide	No								

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1	Int			Add				

Read multiply operands? DIVD could have been issued on this cycle.

Scoreboard Example Cycle 8a

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	
MULTD	F0	F2	F4	6			
SUBD	F8	F6	F2	7			
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2				

Clock 8

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	Yes	Load	F2		R3				Yes
Mult1	Yes	Mult	F0	F2	F4	Int		No	Yes
Mult2	No								
Add	Yes	Sub	F8	F6	F2		Int	Yes	No
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1	Int			Add	Div			

Scoreboard Example Cycle 8b

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	8
MULTD	F0	F2	F4	6			
SUBD	F8	F6	F2	7			
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2				

Clock 8

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	No								
Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Sub	F8	F6	F2			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1				Add	Div			

Scoreboard Example Cycle 9

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	8
MULTD	F0	F2	F4	6	9		
SUBD	F8	F6	F2	7	9		
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2				

Clock 9

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	No								
Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Sub	F8	F6	F2			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1				Add	Div			

Issue ADDD?

Scoreboard Example Cycle 11

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	8
MULTD	F0	F2	F4	6	9		
SUBD	F8	F6	F2	7	9	11	
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2				

Clock 11

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	No								
Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Sub	F8	F6	F2			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1				Add	Div			

Scoreboard Example Cycle 12

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	8
MULTD	F0	F2	F4	6	9		
SUBD	F8	F6	F2	7	9	11	12
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2				

Clock 12

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	No								
Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
Add	No								
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1					Div			

Scoreboard Example Cycle 13

Instruction status

Instruction		j	k	Issue	Read operands	Execution complete	Write Result
LD	F6	34	R2	1	2	3	4
LD	F2	45	R3	5	6	7	8
MULTD	F0	F2	F4	6	9		
SUBD	F8	F6	F2	7	9	11	12
DIVD	F10	F0	F6	8			
ADDD	F6	F8	F2	13			

Clock 13

Functional unit status

Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Integer	No								
Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
Mult2	No								
Add	Yes	Add	F6	F8	F2			Yes	Yes
Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

	F0	F2	F4	F6	F8	F10	F12	...	F30
FU	Mult1			Add		Div			