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Chapter 4
Bipolar Junction Transistor (BJT) DC Analysis

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Course Learning Outcomes

1. Apply the basic law and theorems of electronic devices to describe their basic operation.

2. Apply the basic law, theorems and methods of analysis to solve complex problem related to circuitry.

3. Work in a team and communicate effectively.

Learning Outcomes

i. Describe the basic structure of a BJT.

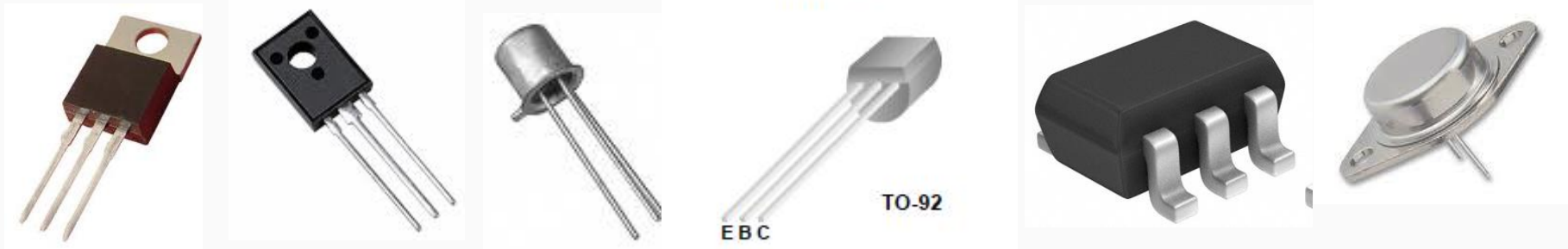
ii. Explain and analyze basic BJT bias and operation.

iii. Discuss on the function of a BJT as an amplifier.

iv. Discuss the parameters and characteristic of a BJT and its application in electrical circuit.

What is Transistor?

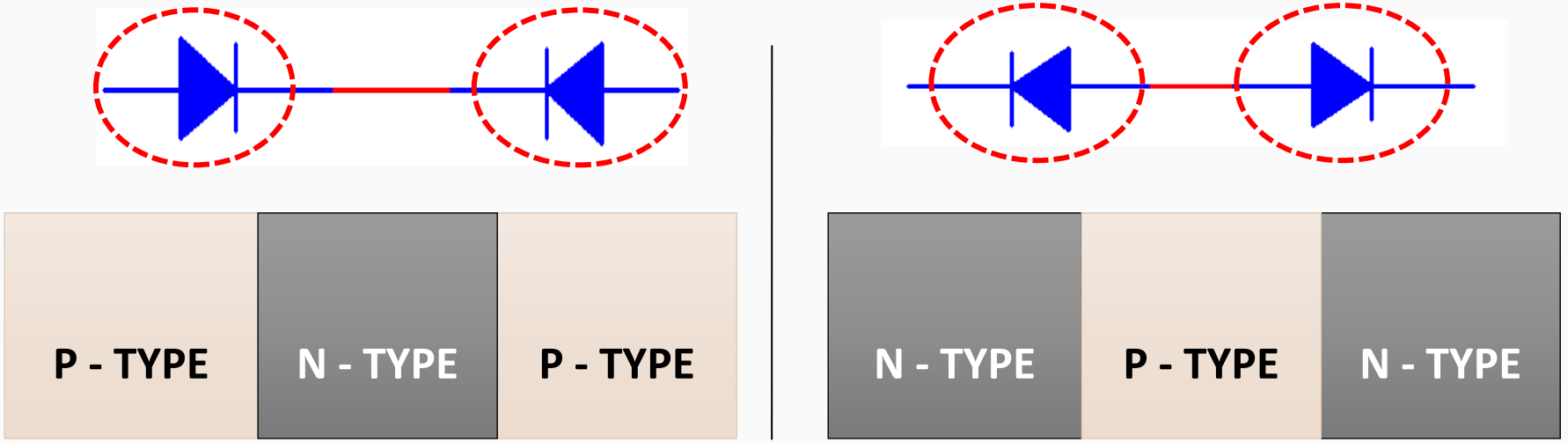
- Transistors are solid state devices that is used for amplifying, controlling and generating electrical signal.



- Transistors are used widely in electronic equipment such as computers, calculators, radios and communication satellite.

What is Transistor?

- Two basic types of transistor is bipolar junction transistor (BJT) and Field Effect Transistor (FET).
- Transistor is like 2 diodes connected.



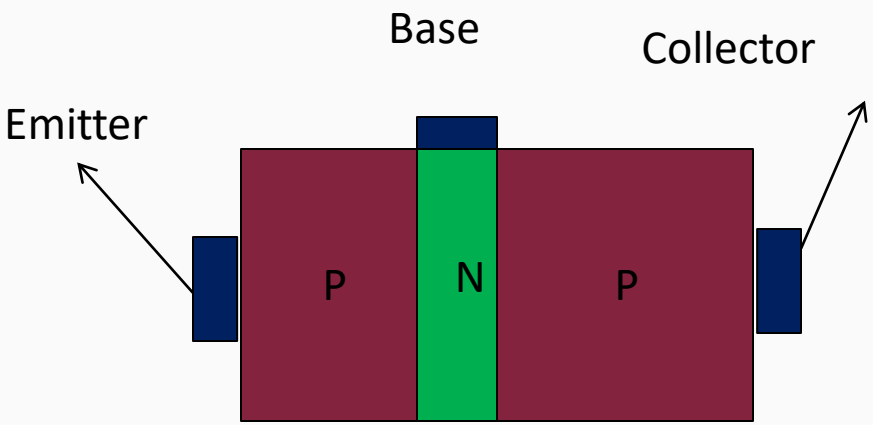
- Each region have different doping concentration.
- Transistor is widely been used as switch and amplifier.

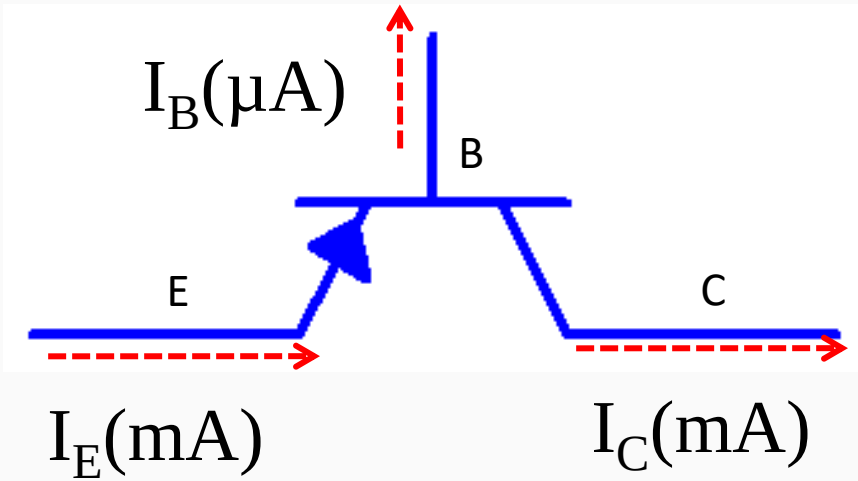
Introduction to BJT

- BJT is bipolar because both majority and minority carriers take part in the current flow. (a) N-type - electrons as majority carrier (b) P-type – holes as majority carrier.
- 2 types of BJT: (a) NPN and (b) PNP
- BJT regions are:
  - Emitter (E) – send the carries into the base region and then into the collector.
  - Base (B)act as control region. Carriers flow depending on the biased voltage.
  - Collector (C) – collects the carries.

Structure & Symbol of BJT

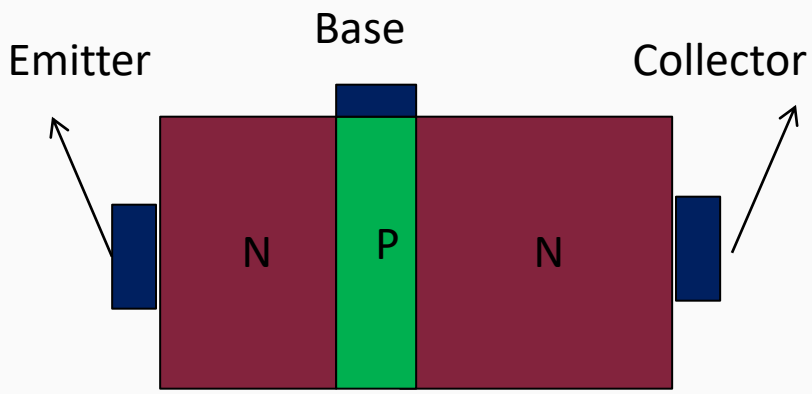
PNP TYPE

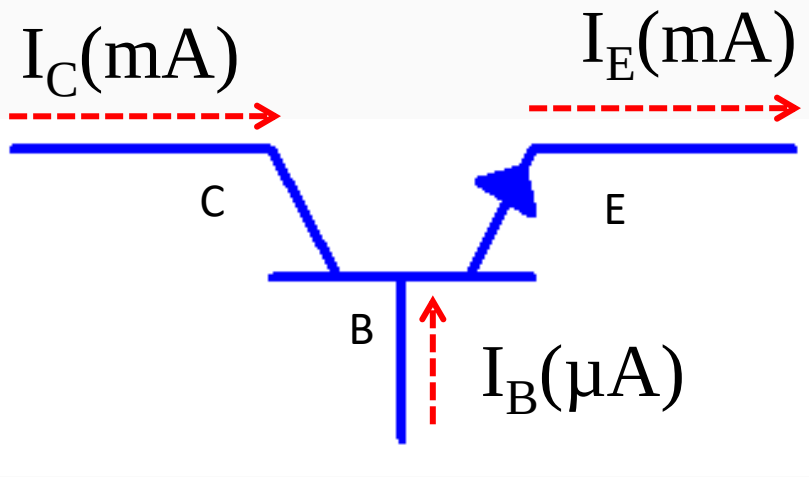




$I_E = I_C + I_B$

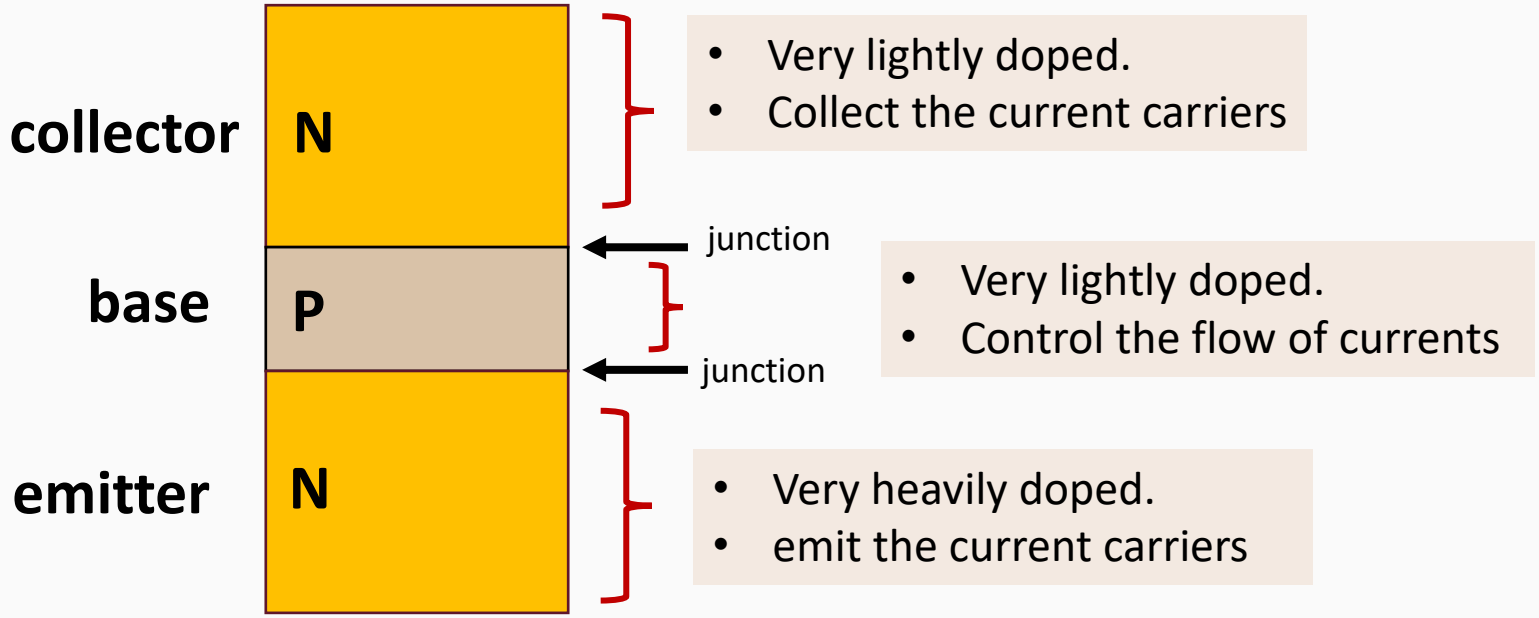
NPN TYPE





$I_E = I_C + I_B$

NPN Transistor Structure



- The emitter is rich in current carriers. It send the carriers into the base region and on to the collector.
- The collector collect the carriers.
- The emitter emits the carriers.
- The base act as a control region. It can allow none, some or many carriers to flow from emitter to collector.

BJT Characteristic & Parameters

- β_{DC} – is the ratio of the DC collector current, I_C to the DC base current, (I_B)
- Typical value range from less than 20 to 200 or higher.

$$\beta_{DC} = \frac{I_C}{I_B}$$

- α_{DC} – is the ratio of the DC emitter current, I_E to the DC collector current, (I_C).
- The value range from 0.95 to 0.99 but always less than 1.

$$\alpha_{DC} = \frac{I_C}{I_E} \qquad \beta = \left(\frac{\alpha}{1-\alpha}\right)$$

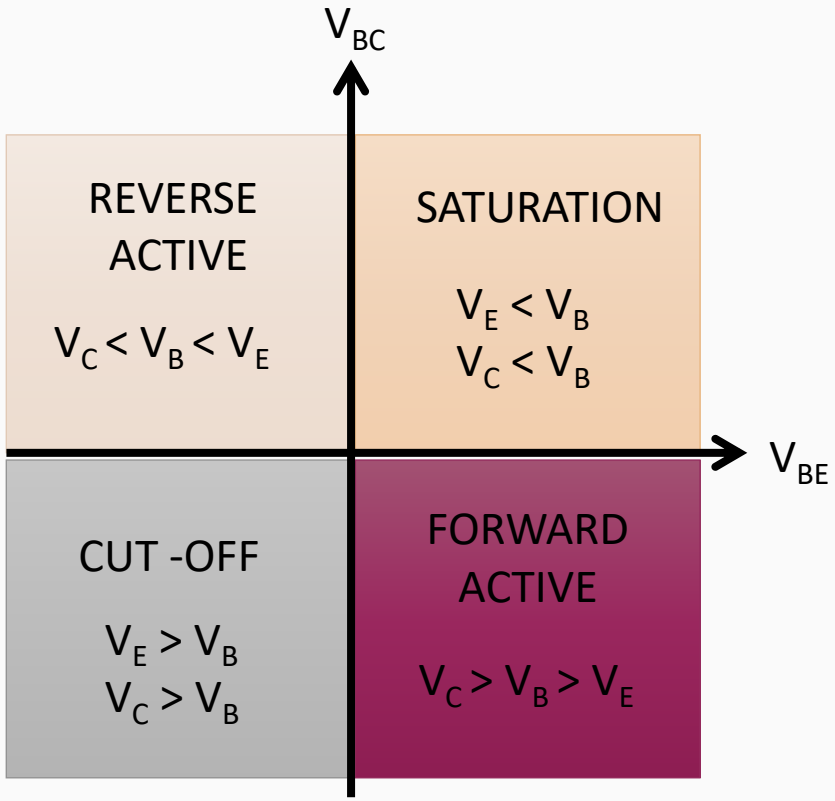
BJT Behavior: Current-Voltage Characteristics

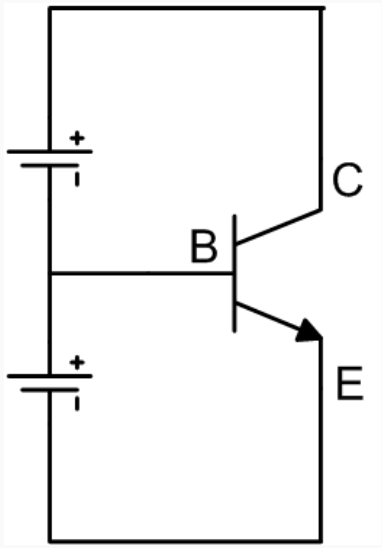
- The behaviour of the transistor can be represented by current-voltage (I-V) curves (called the characteristic curves of the device).
- **Input Characteristics**
  - The relation between **input current** and **input voltage** for different values of **output voltage**
- **Output Characteristics**
  - The relation between **output current** and **output voltage** for different values of **input current**

BJT Basic Operation Region

- To produce a desired mode of operation, the two P-N junctions must be correctly biased
- NPN transistor will be used for illustrationThe operation of the PNP is the same as for the NPN except that
  - the roles of the electrons and holes
  - the bias voltage polarities
  - the current directions - are all reversed
- A single PN junction has two different types of bias: forward and reverse.
- Thus, a 2 PN junction device has four types of bias.

BJT Mode of Operation for NPN and PNP





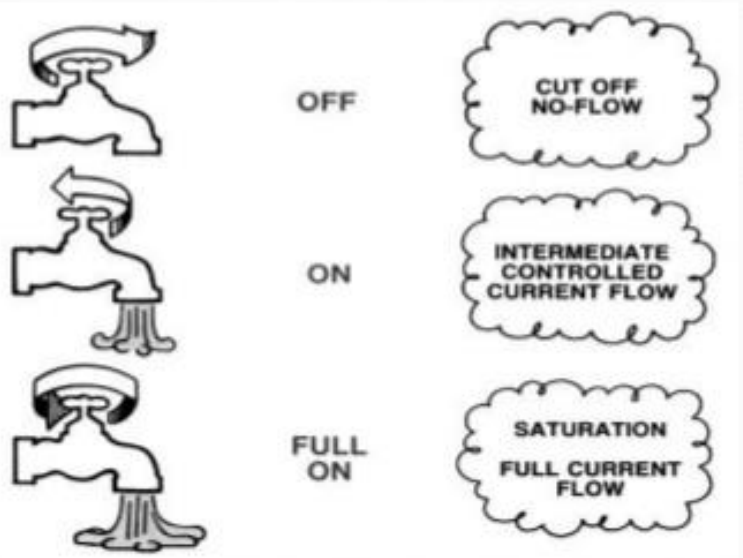
- Saturation and cut-off operations are important for digital circuits like switching.
- Active region are important for amplifier application.

Operating regions of BJT

Cut-off region

Saturation region

Active region



Example – NPN Transistor

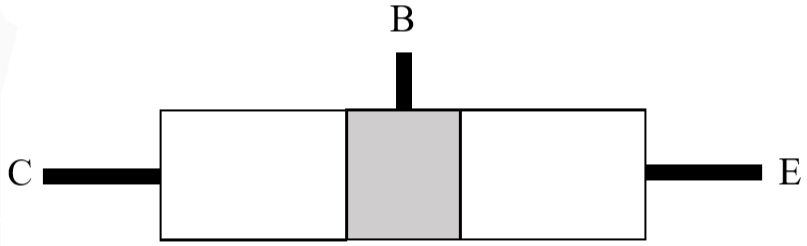
Base -Emitter Junction	Base - Collector Junction	Operating Region
Reverse biased	Reverse biased	
Forward biased	Reverse biased	
Forward biased	Forward biased	

- What are the two (2) main applications of BJT?

Exercise - https://padlet.com/nurnajahatulhuda/hba67po8p9ok8oun

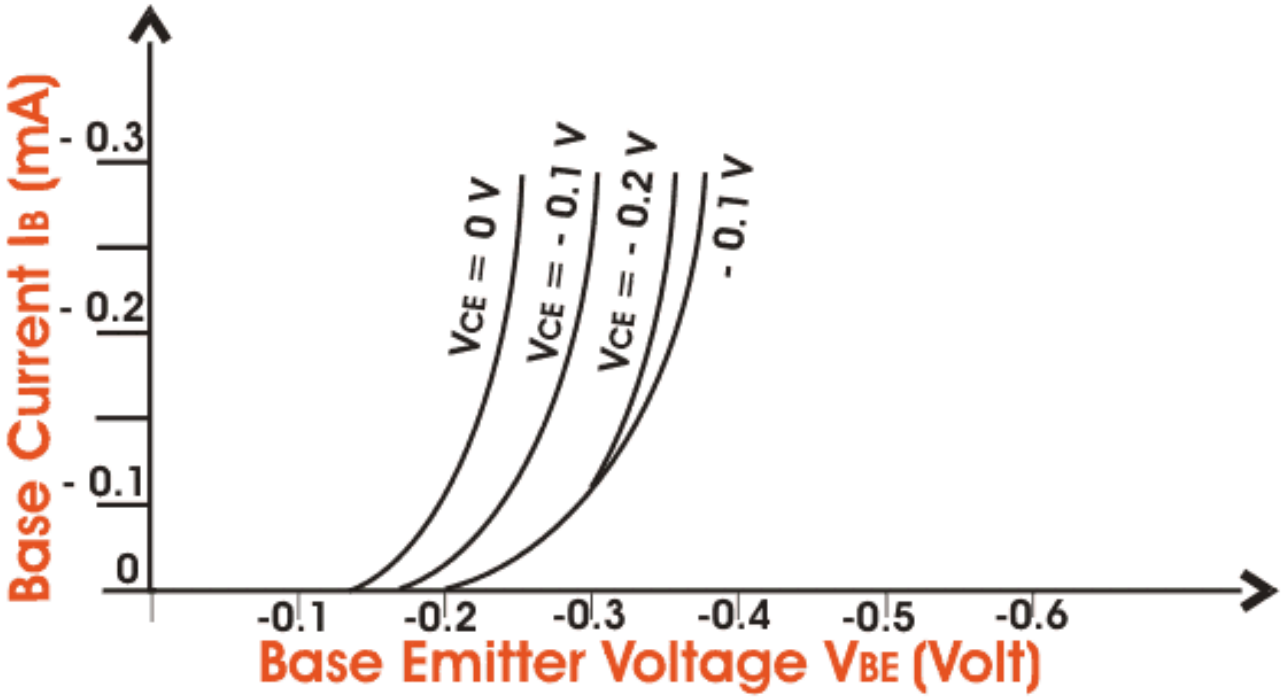
Figure below illustrate a structure of NPN transistor contain collector (C), base (B) and emitter (E). Fill in the blank.

- The base (B) to emitter (E) junction is normally _____ biased and the resistance at the junction is _____.
- The collector (C) to base (B) junction is normally _____ biased and the resistance at the junction is _____.
- The smallest current in NPN bipolar junction transistor is the _____ current.

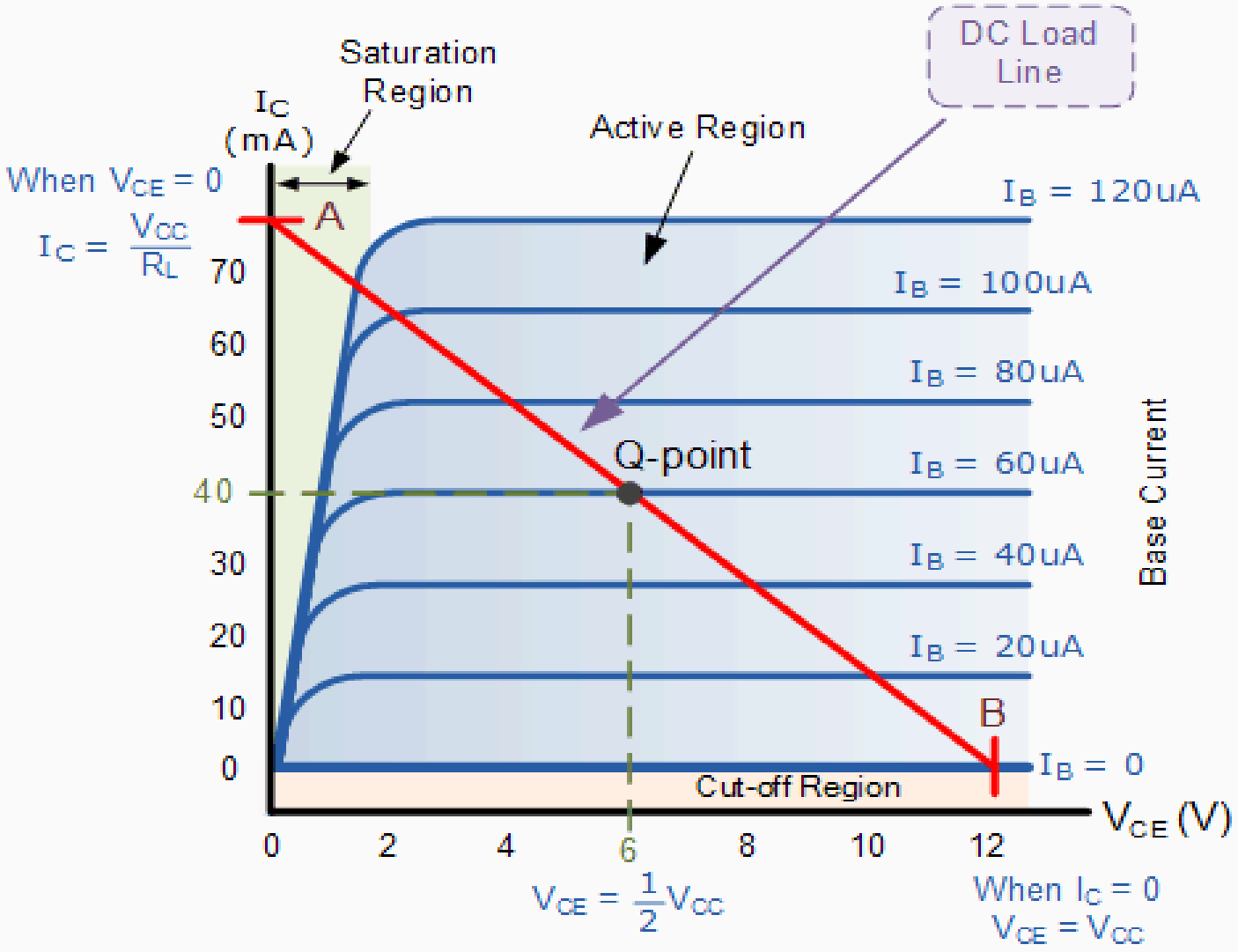


Collector - Base Characteristic Curve Input Characteristic

- The characteristic resembles a family of forward biased diode curves
- I_B increases as V_{CE} decreases for a fixed value of V_{BE}



Collector Characteristic Curve Output Characteristic



BJT Region Comparison

Active Region	Saturation Region	Cut – Off Region
❑ B-E junction forward biased	❑ B-E and C-E junction are forward biased.	❑ B-E and C-E junction are reverse biased.
❑ C- B junction reverse biased	❑ I_B and I_C are too big but V_{CE} is very small.	❑ I_B < μA but I_C is not zero. Avoid this region for undistorted signal.
❑ Can be employed to used as voltage and current amplification	❑ Suitable region to used as logic switch.	❑ Suitable region to used as logic switch.

What is Q – Point? (DC Operating Point)

- When the BJT only have DC input (no ac input) it will have specific value of I_C and V_{CE}.
- It correspond on the specific point on the DC load line. This point is called Q – point.
- It's a point on the collector characteristic curve (I_C – V_{CE}) with constant I_B.

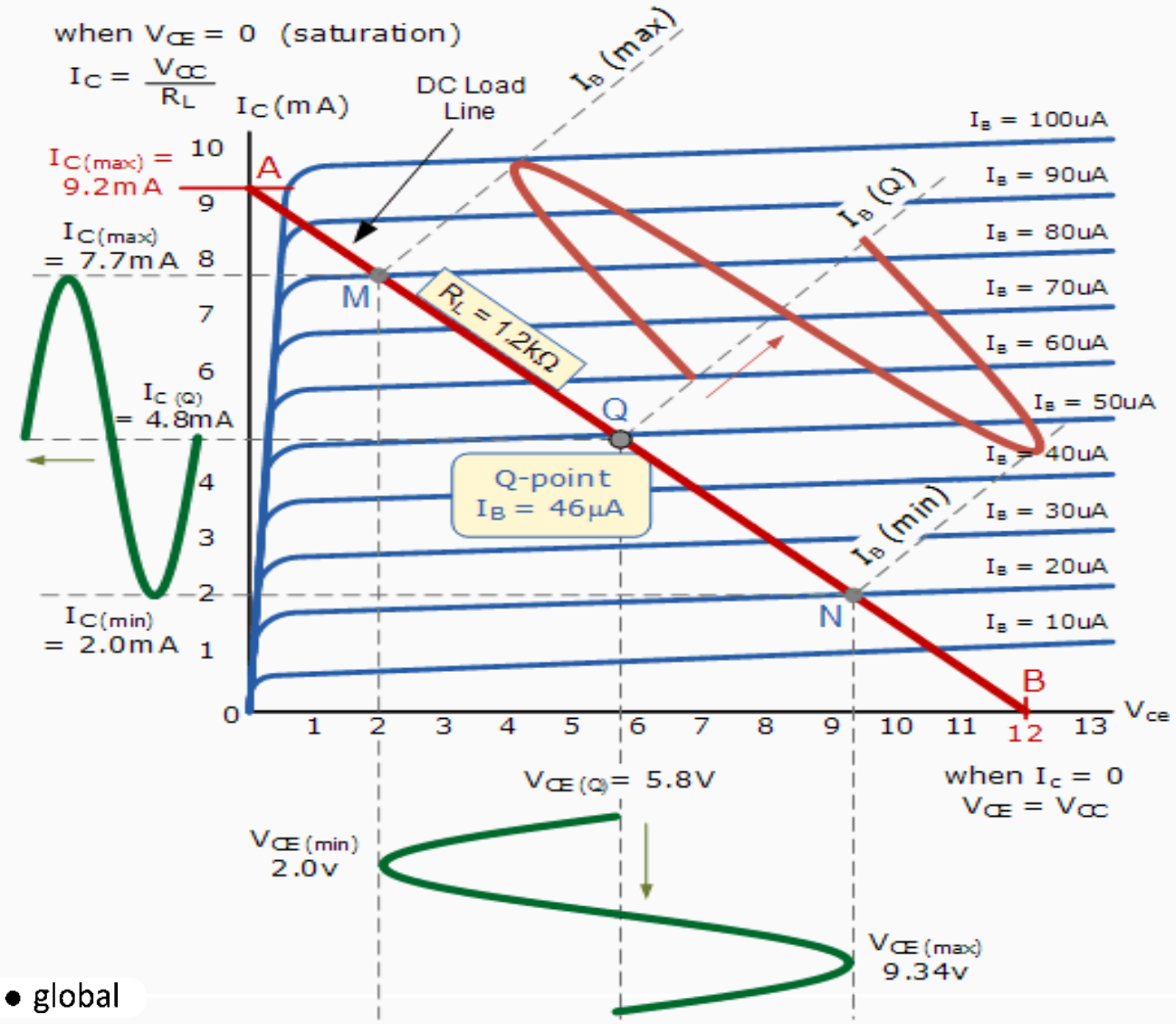
Purpose of BJT Biasing

BJT should be biased to determine its operating point or Q point.

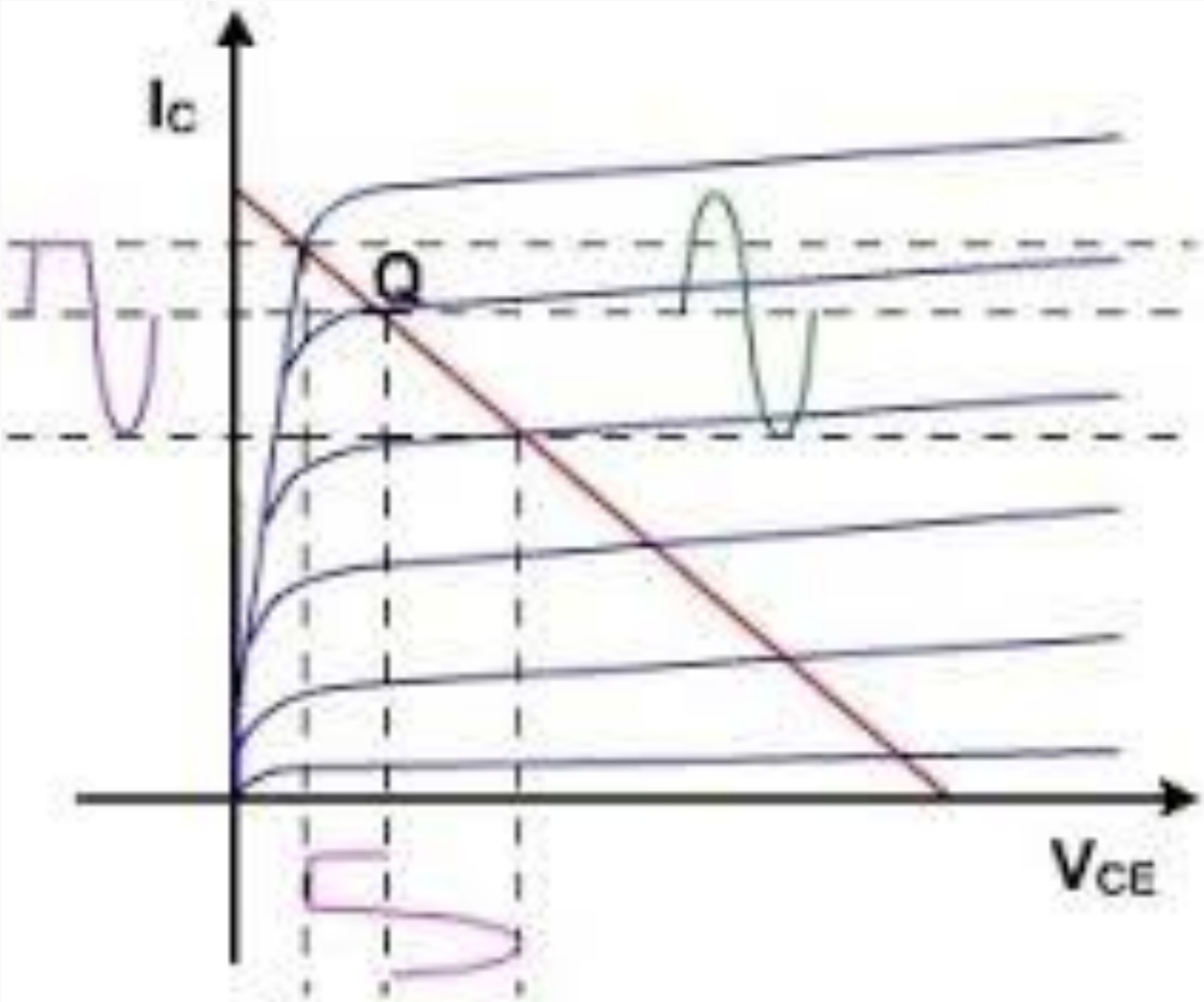
To ensure whether it is in active region to be used as amplifier or in saturation or cut-off region to be used as switch.

A good biasing circuit must have Q – point at the center of the DC load line to obtain maximum symmetrical output swing.

Q – Point at the center of DC Load line



Q – Point NOT at the center of DC Load line



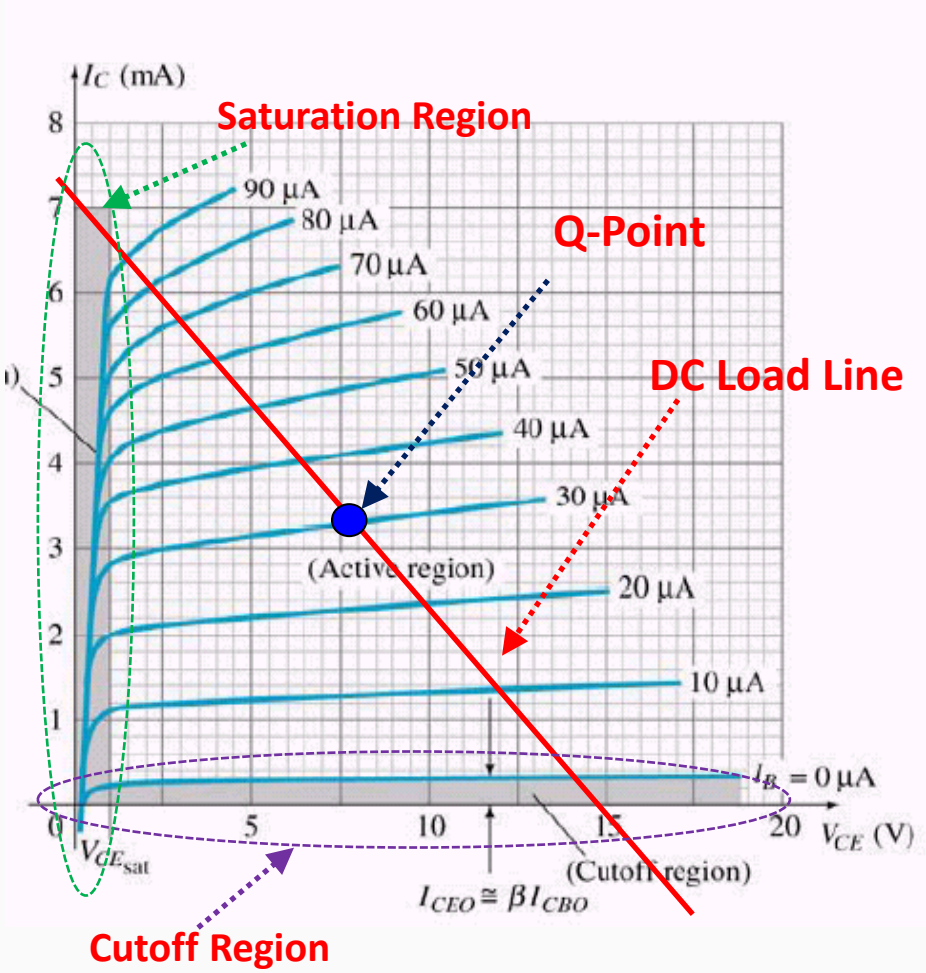
BJT DC Load Line

- A straight line intersecting the vertical axis at approximately $I_{C(sat)}$ and the horizontal axis at $V_{CE(off)}$.
- $I_{C(sat)}$ occurs when transistor operating in *saturation region*

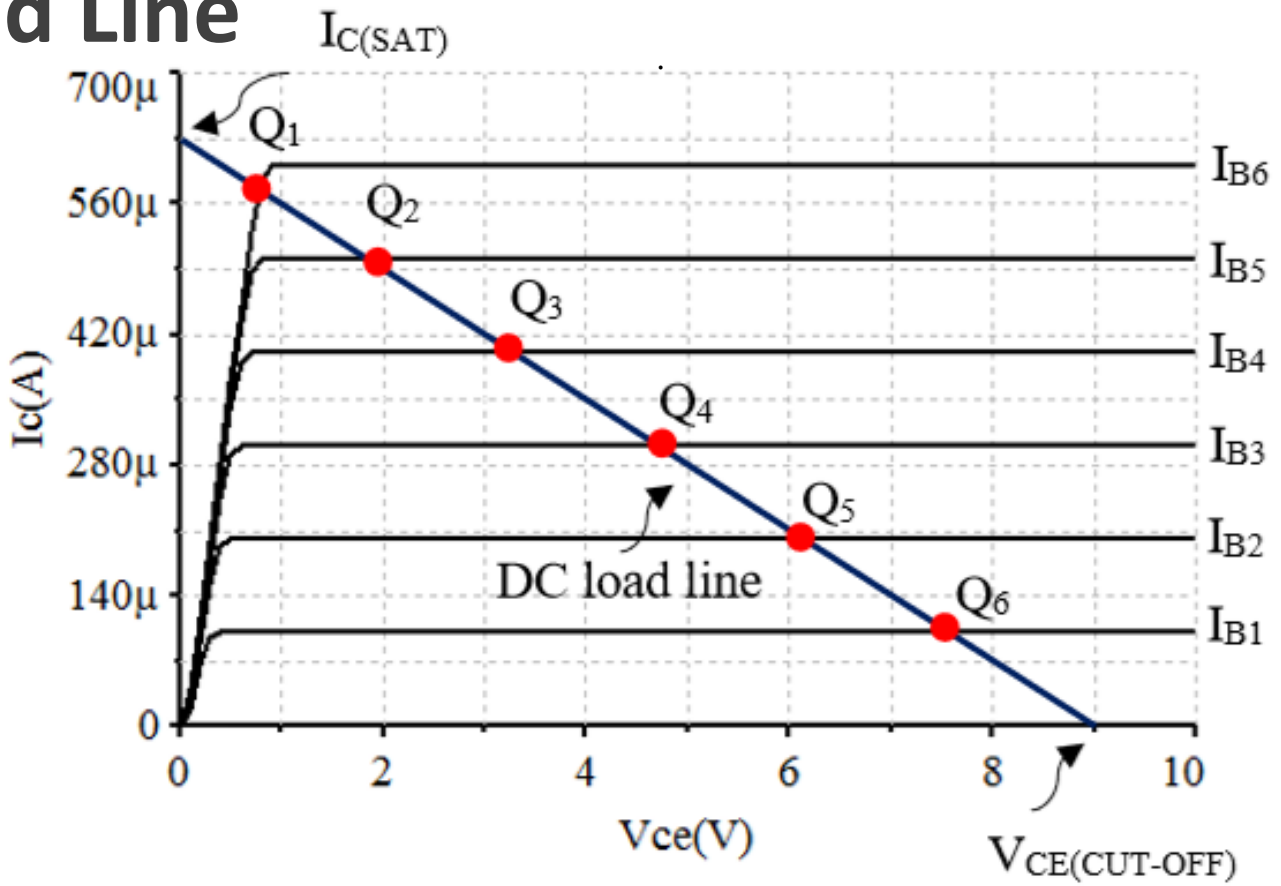
$$I_{C_{sat}} = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0}$$

- $V_{CE(off)}$ occurs when transistor operating in *cut-off region*

$$V_{CE_{(off)}} = V_{CC} - I_C R_C\Big|_{I_C=0}$$



BJT DC Load Line



To make sure that the chosen Q –point is useful for amplifier application, the Q-point, it is best located at the canter of the DC load line where:

$$I_{CQ} = \frac{1}{2} I_{C(SAT)} \text{ and } V_{CEQ} = \frac{1}{2} V_{CC}$$

Exercise

Referring to the output characteristic shown, identify the operation region if :

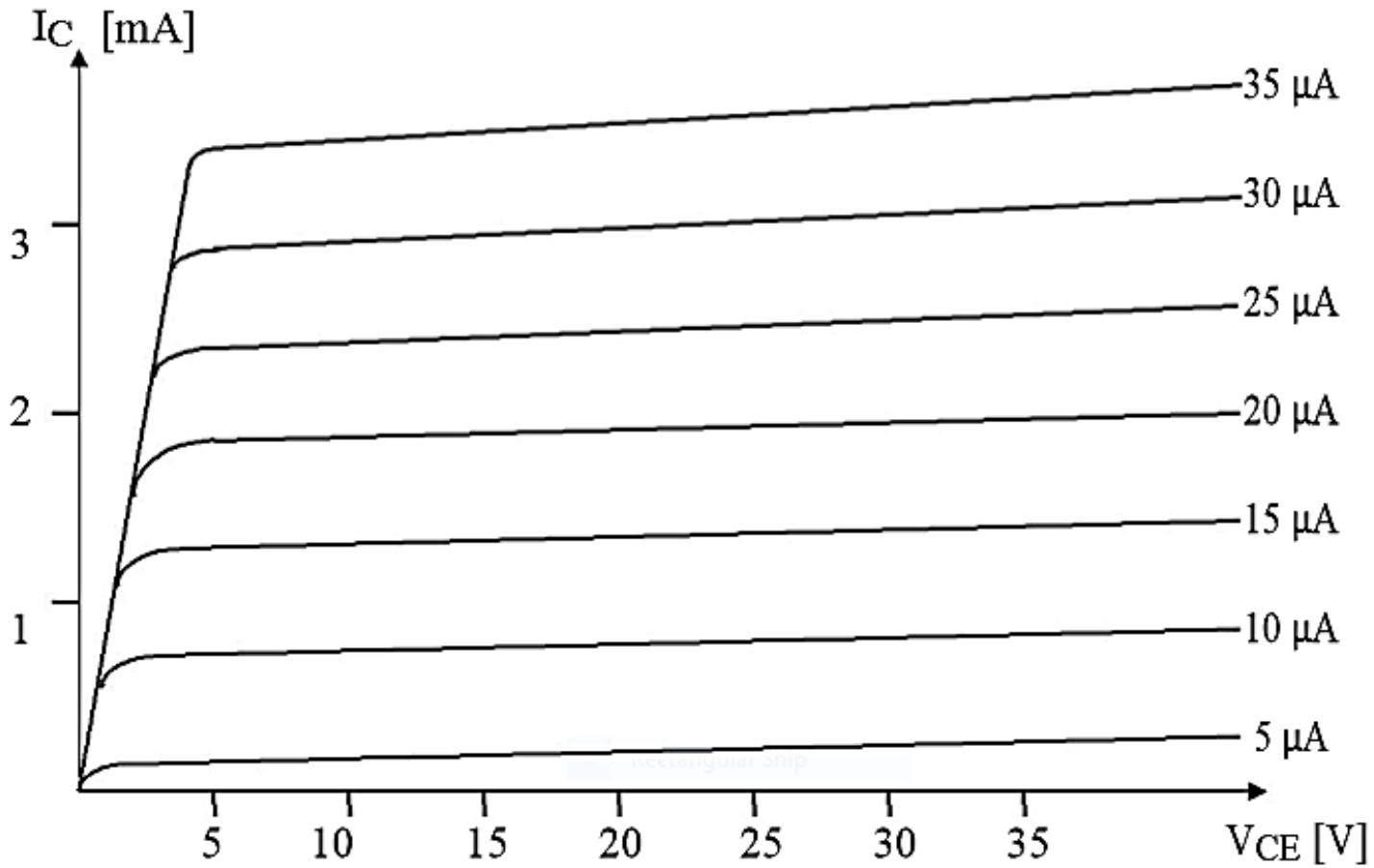
(a) $I_C = 3mA$ $V_{CE} = 15V$

(b) $I_C = 2.5mA$ $I_B = 35\ \mu A$

(c) $I_B = 10\ \mu A$ $V_{CE} = 8V$

(d) $I_B = 0$ $V_{CE} = 8V$

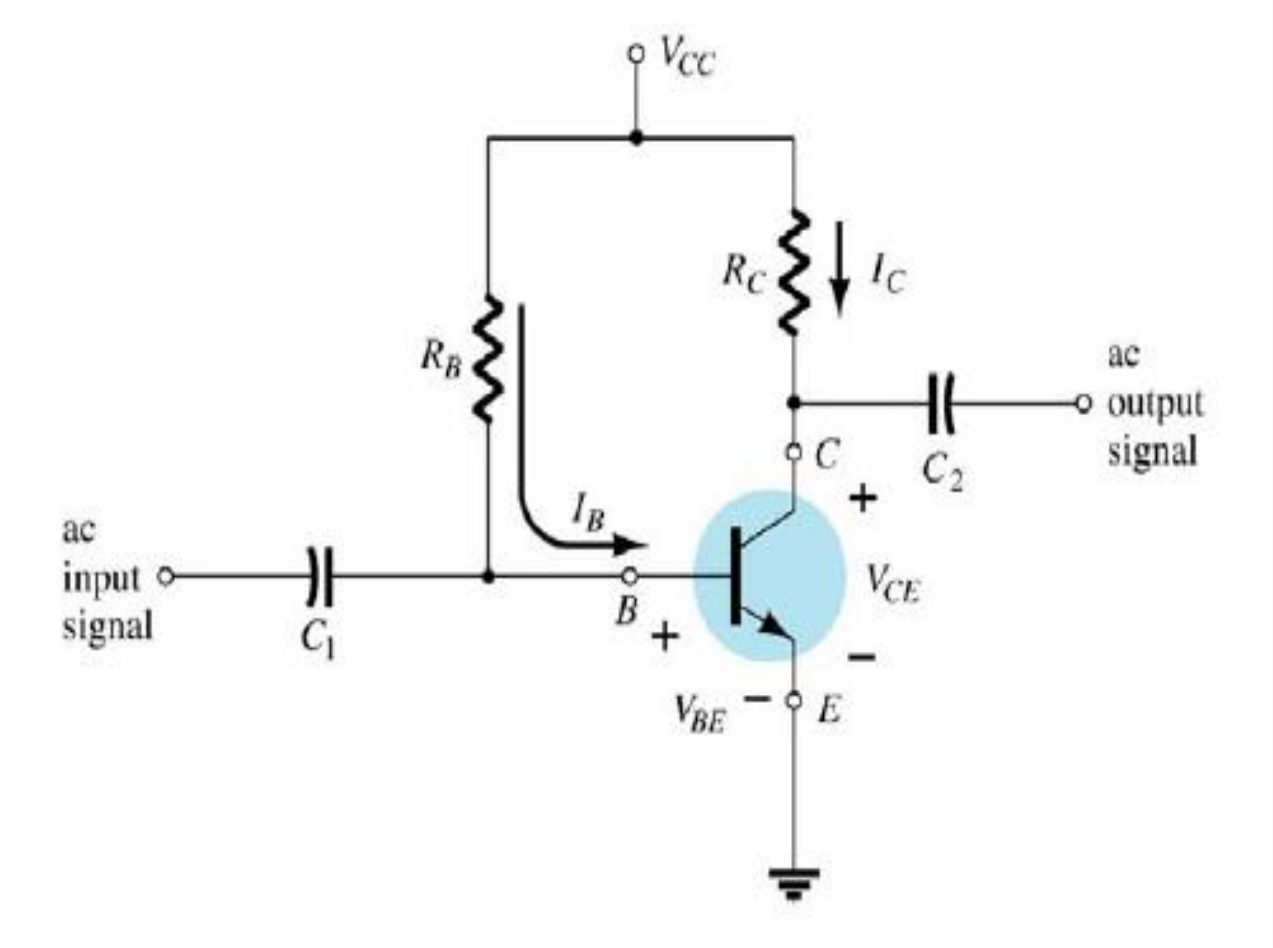
(d) $I_B = 20\ \mu A$ $V_{CE} = 0.2V$



Main Types of BJT Biasing Circuit

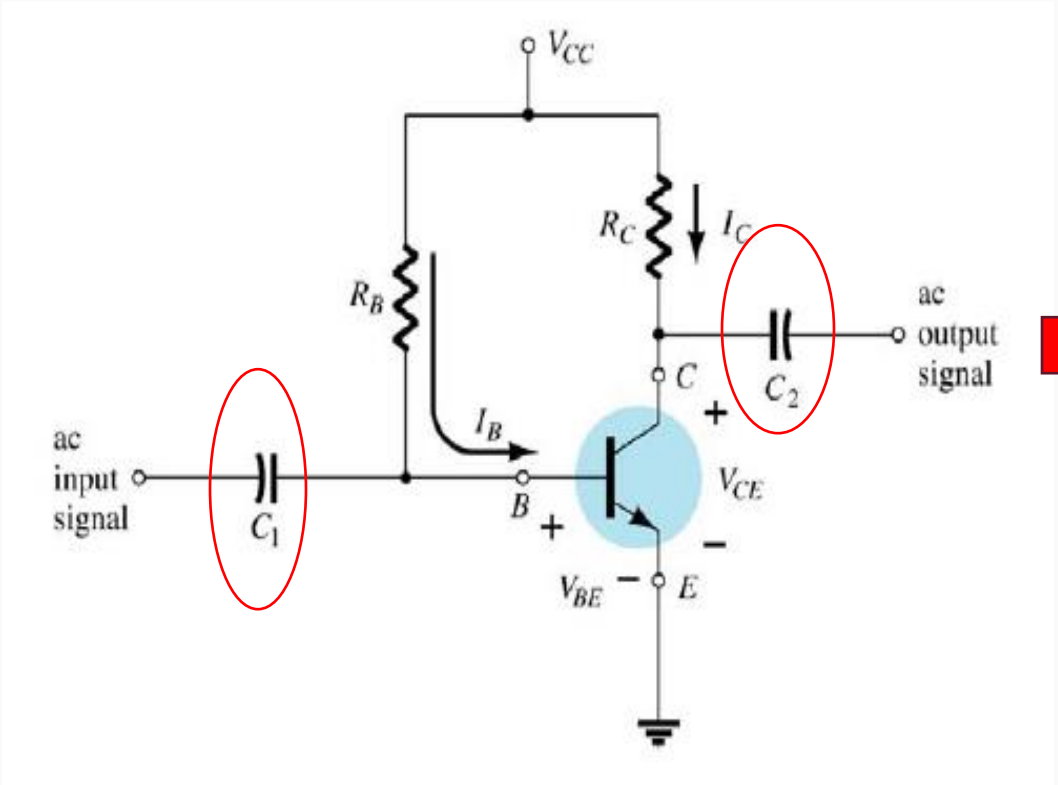
- Fixed Base Bias Circuit
- Fixed Base Bias with emitter resistor (Emitter stabilized bias circuit)
- Voltage-Divider Bias Circuit

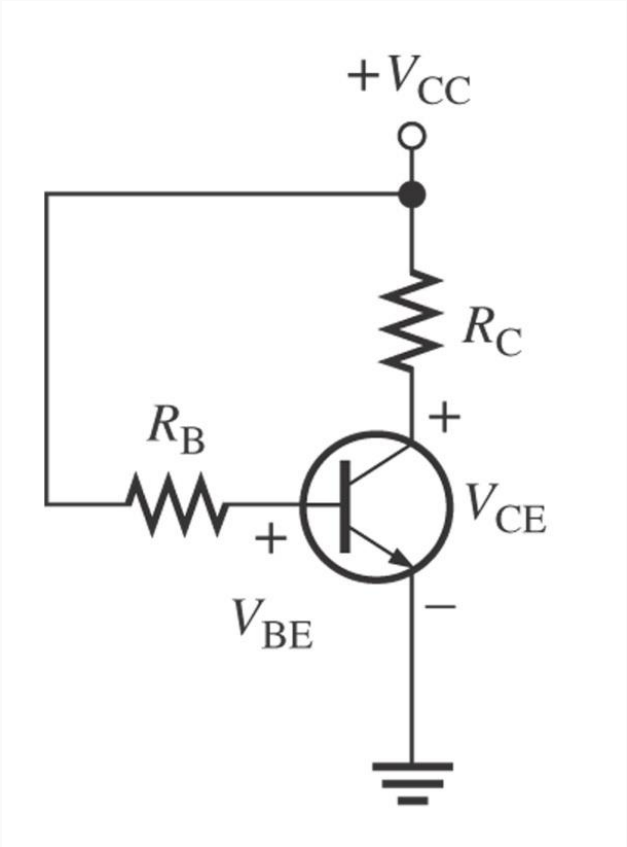
BJT Circuit Analysis: Fixed Bias Circuit



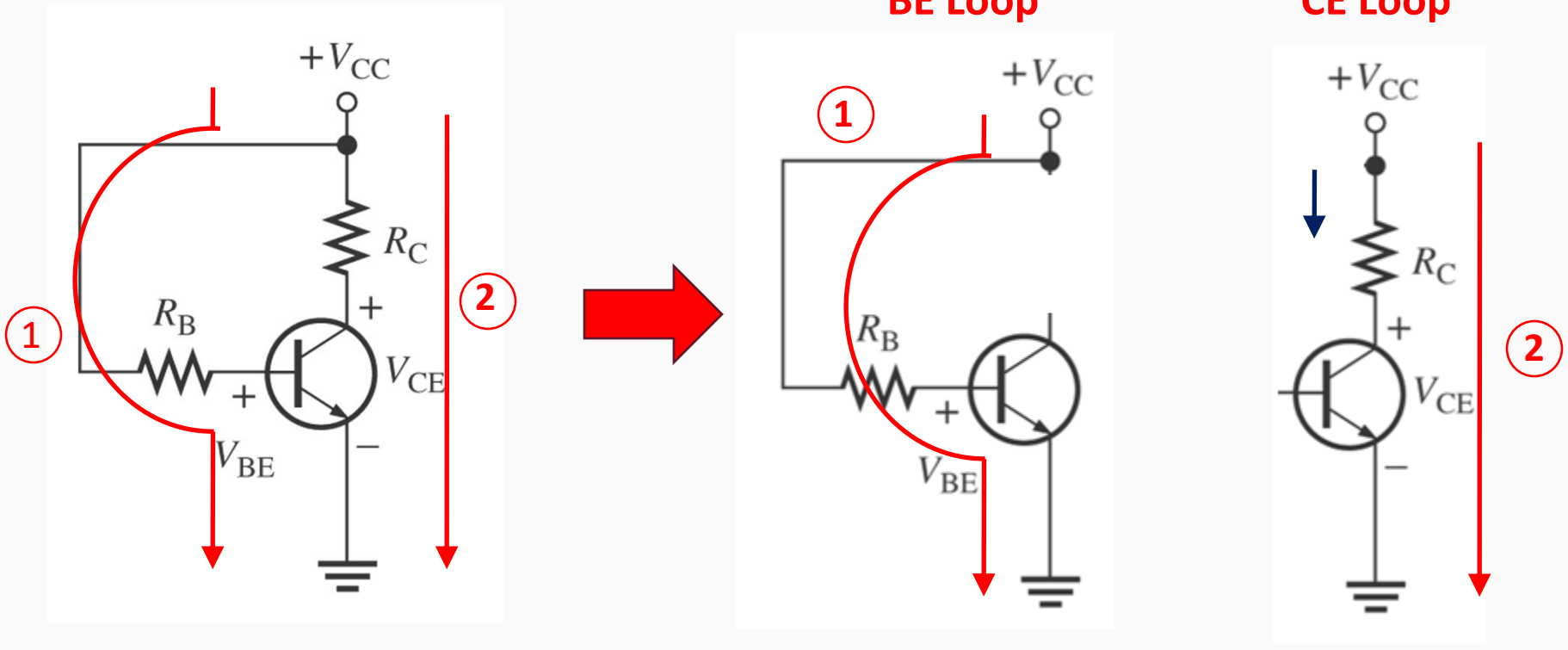
- This is common emitter (CE) configuration
- Solve the circuit using HVK
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop
  - CE loop

1st step: Locate capacitors and replace them with an open circuit

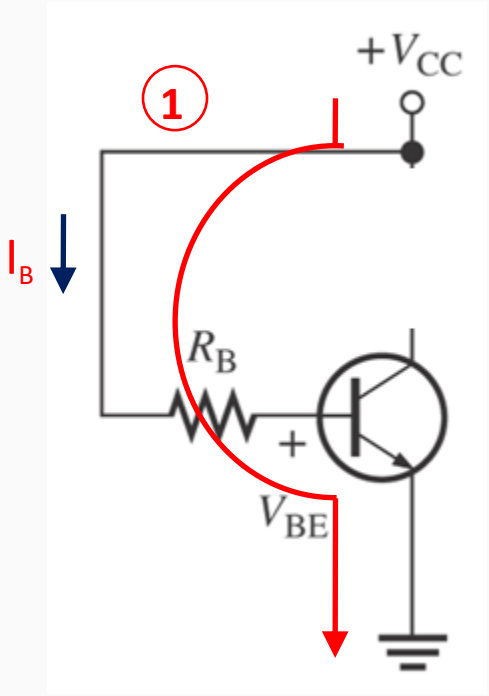




2nd step: Locate 2 main loops



BE Loop Analysis

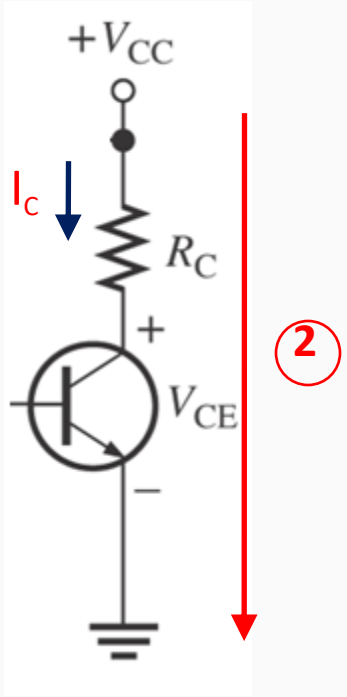


- From HVK;

$$V_{CC} - I_B R_B - V_{BE} = 0 \quad \text{(A)}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

CE Loop Analysis



- From HVK;

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

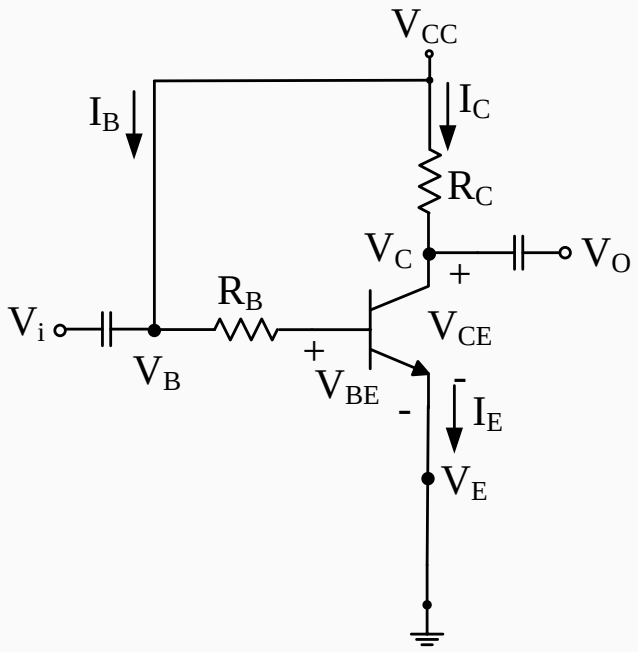
- As we known;

- Substituting (A) with (B)

$$I_C = \beta I_B \quad (B)$$

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

BJT Circuit Analysis: Fixed Bias Circuit



- Taking the Kirchhoff voltage law (KVL) around the B – E loop yield the following equation:

$$V_{CC} - I_B R_B - V_{BE} = 0$$

- Solving for I_B

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

- The collector current I_C is then given by

$$I_C = \beta I_B = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

- The voltage at the base, collector and emitter can be calculated using

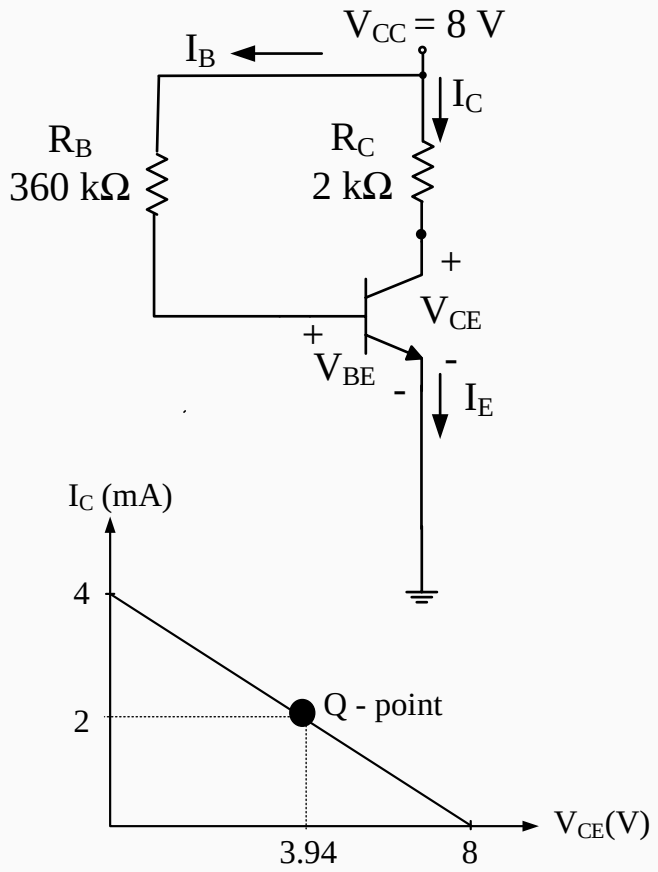
$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_B R_B$$

- I_C is directly dependent on β. This is unfavourable since β varies with temperature and I_C. When I_C is changing, it cause V_{CE} to change. This will change the Q – point of the transistor and make the fixed base biasing circuit very unstable.

Example : Fixed Biasing Circuit

Draw the DC load line and find I_{BQ}, I_{CQ}, V_{CEQ}, V_{CQ}, V_{EQ} and V_{BQ}.
Comment on the location of the Q – point.



Using C - E Loop:

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{8 - 0.7}{360k} = \underline{20.28\ \mu A}$$

$$I_C = I_{CQ} = \beta I_B = (100)20.28\mu = \underline{2.03mA}$$

Using C - E Loop:

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad .....(A)$$

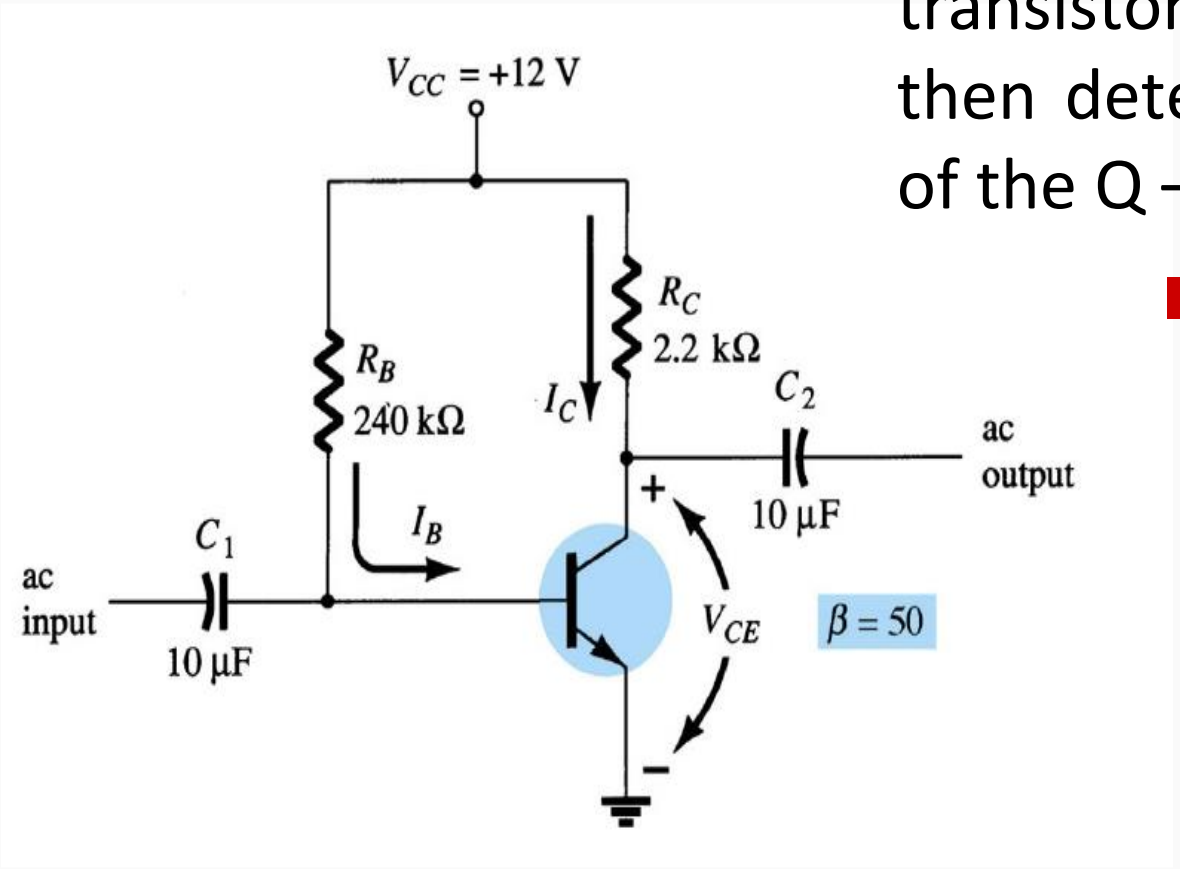
$$V_{CE} = V_{CEQ} = V_{CC} - I_{CQ} R_C = 8 - (2.03m \times 2k) = 3.94\ V$$

when $I_C = 0$, $V_{CE} = V_{CE(CUT\text{-}OFF)} = V_{CC} = 8V$

when $V_{CE} = 0$, $I_C = I_{C(SAT)} = \frac{V_{CC}}{R_C + R_E} = \frac{8}{2k} = 4\ mA$

** The Q – point is in the active region. Therefore this biasing circuit is suitable to be used in amplifier.

Example : Fixed Bias Circuit



- Find I_C, I_B, V_{CE}, V_B, V_C, V_{BC}? (Silicon transistor) Construct the DC load line then determine the operation region of the Q – point.
  - Answers;

    IC = 2.35 mA

    IB = 47.08 µA

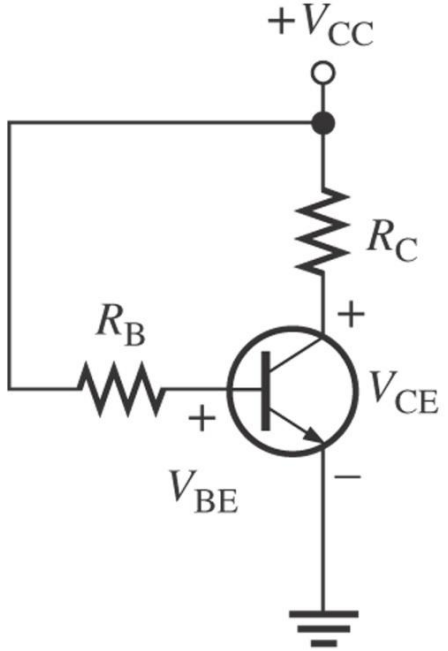
    VCE = 6.83V

    VB = 0.7V

    VC = 6.83V

    VBC = -6.13V

step 1 : open all capacitors and redraw the circuit.



step 2 :

B - E Loop KVL

$$12 - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{12 - V_{BE}}{R_B} = \frac{12 - 0.7}{240k} = \underline{47.1\,\mu A} \quad \surd$$

using relation $I_E = (1+\beta) I_B$ and $I_E \approx I_C$

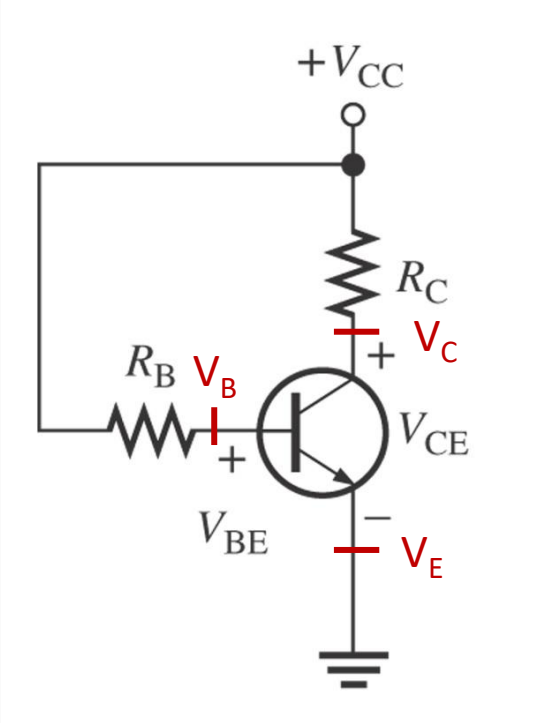
$$I_E \approx I_C = (1+50) \times 47.1\,\mu = \underline{2.40\,mA} \quad \surd$$

step 3

C - E Loop KVL

$$12 - I_C R_C - V_{CE} = 0$$

$$V_{CE} = 12 - I_C R_C = 12 - (2.40\,m \times 2.2k) = \underline{6.72V} \quad \surd$$



From the circuit, $V_E = 0V$. √

it is known that $V_{BE} = 0.7V$

$$V_{BE} = V_B - V_E$$

$$\therefore V_B = V_{BE} = \underline{0.7\,V} \quad \surd$$

at the collector (C) terminal :

$$V_{CE} = V_C - V_E \quad \text{and } V_E = 0V$$

$$\therefore V_C = V_{CE} = \underline{6.72\,V}$$

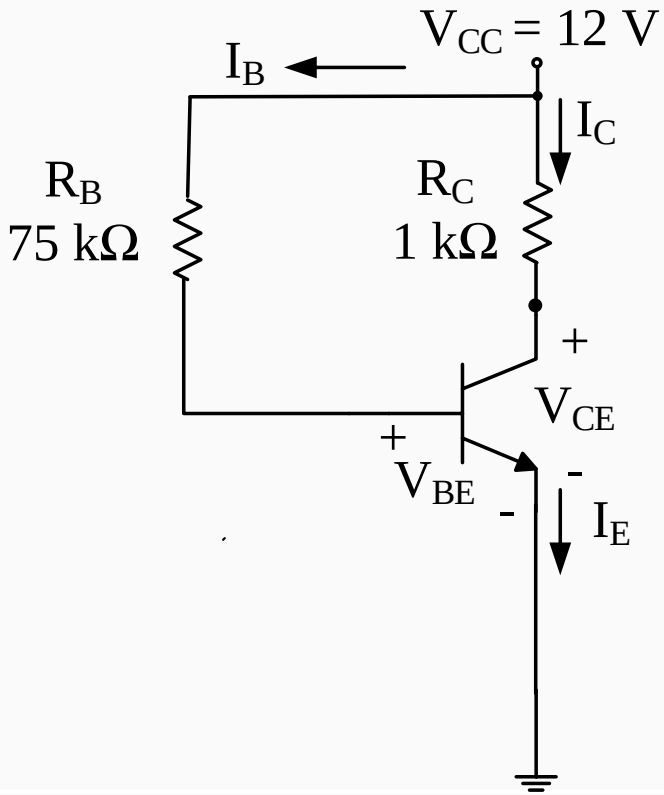
at the base (B) terminal :

$$V_{BC} = V_B - V_C$$

$$V_{BC} = V_B - V_C = 0.7 - 6.72 = \underline{-6.02\,V} \quad \surd$$

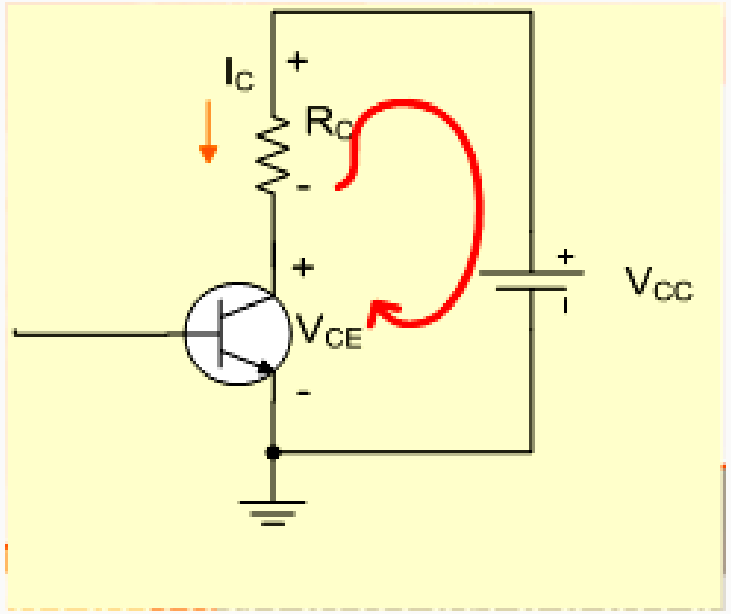
Exercise : Fixed Bias Circuit

For the biasing circuit shown, determine the Q – point (I_{CQ}, V_{CEQ}) and confirm its operation region. Construct the DC load line and evaluate the location of the Q – point. Given β = 100. Redo if β is changed to 129.



Load Line Analysis – Fixed Bias Circuit

- We investigate how the actual Q-point is determined.
- Referring to the figure below (output loop), a straight line can be drawn at the output characteristics curve. This line is called the load line.
- This line connects each separate Q-point.
- At any point along the load line, values of I_B, I_C and V_{CE} can be picked from the graph.
- The process to plot the load line are as follows:



Load Line Analysis – Fixed Bias Circuit

- Step 1:

  Apply KVL at output loop, $V_{CE} = V_{CC} - I_C R_C$ (1)

  Choose $I_C = 0$ mA. Substitute into (1), we get

  $V_{CE} = V_{CC}$ (2) → intersects the x-axis

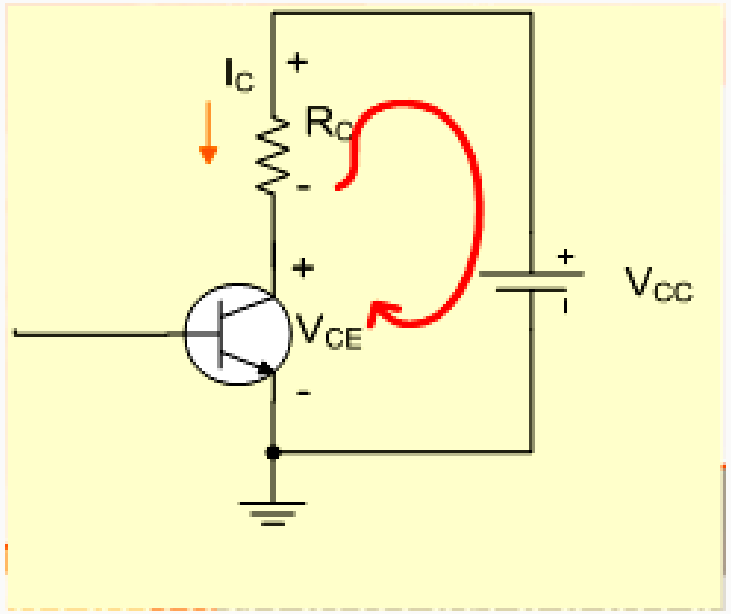
- Step 2:

  Choose $V_{CE} = 0$V and substitute into (1), we get

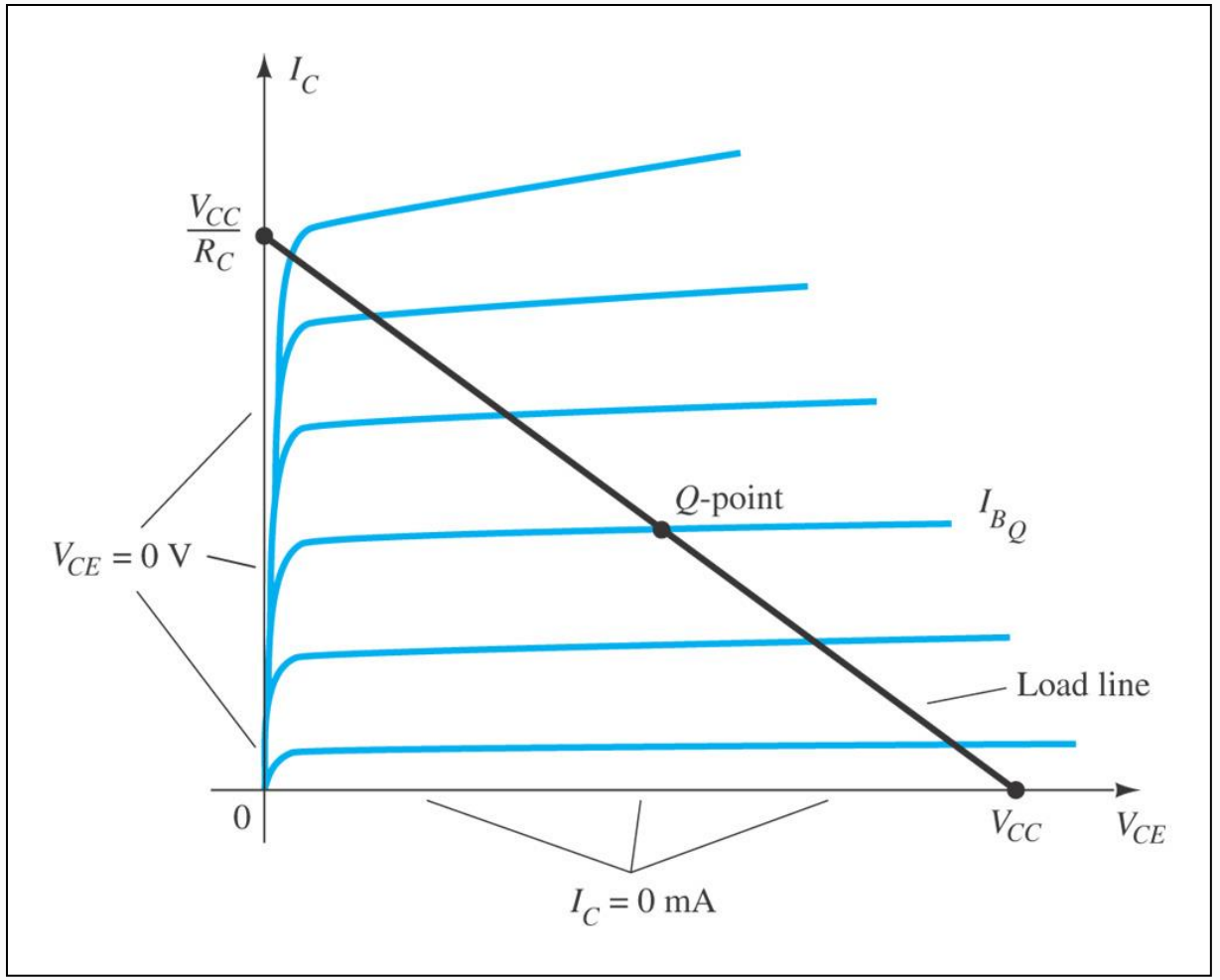
  $I_C = V_{CC}/R_C$ (3) → intersects the y-axis

- Step 3:

  Joining these two points defined by step (2) & (3), we get a straight line that can be drawn as in the next figure.

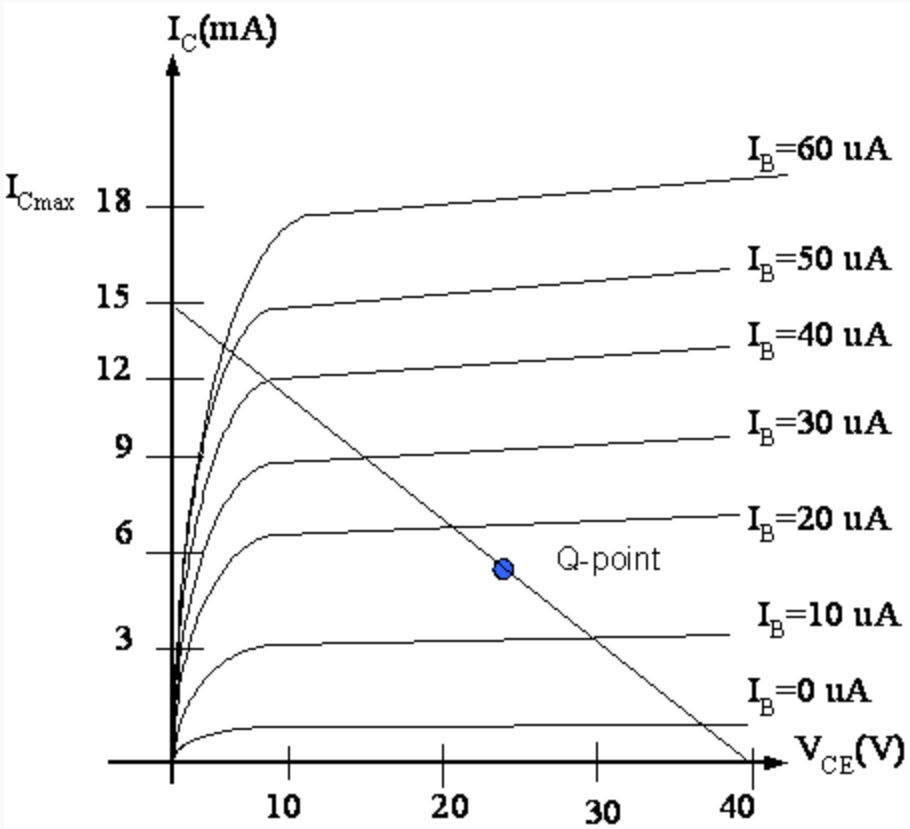


Load Line Analysis – Fixed Bias Circuit



Example

Given the load line in the figure below, define the Q-point & determine the required values of V_{CC}, R_C and R_B for a fixed bias configuration. (Given I_{BQ} at 17 μA)



$$V_{CC} = 40\ \text{V}$$

$$I_C = \frac{V_{cc}}{R_c}$$

$$R_C = \underline{\underline{2.67\ \text{k}\Omega}}$$

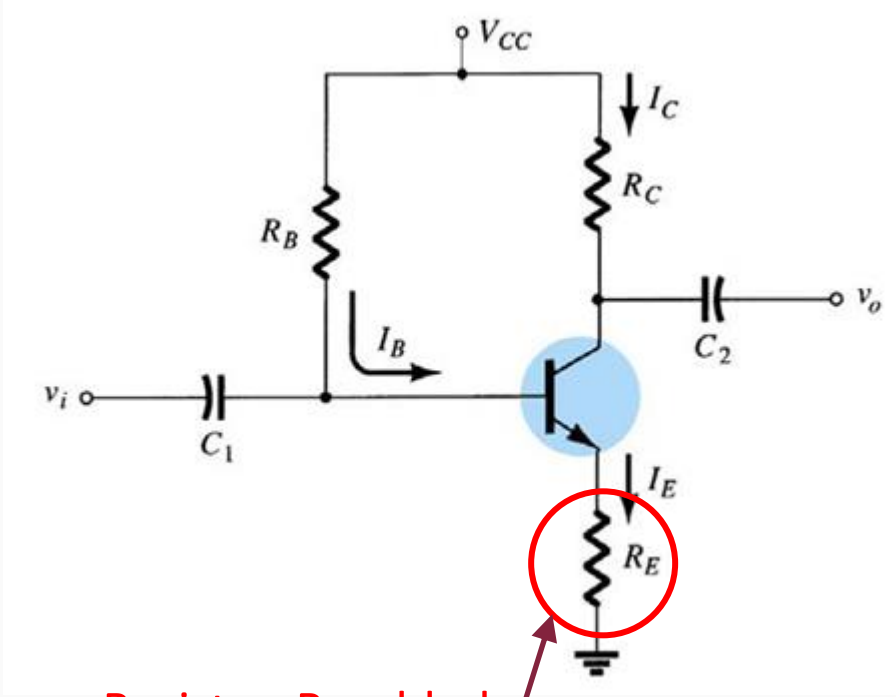
$$\text{at Q-point; } I_B = 17\,\mu\text{A}$$

$$R_B = \underline{\underline{2311\,\text{k}\Omega}}$$

Disadvantages of Fixed Biasing

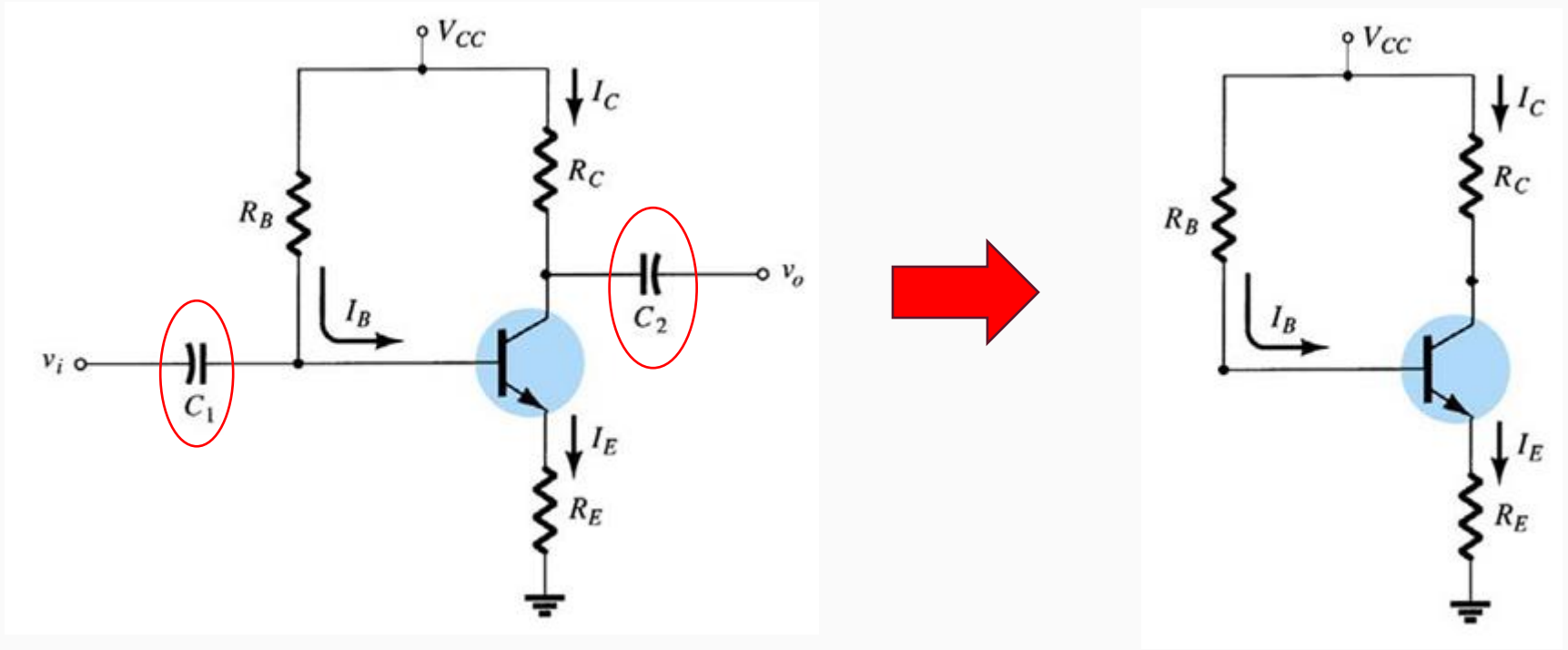
- Unstable – because it is too dependent on β and produce change of Q-point
- For improved bias stability , add emitter resistor to dc bias.

Fixed Bias with emitter resistor (Emitter Stabilized Bias)



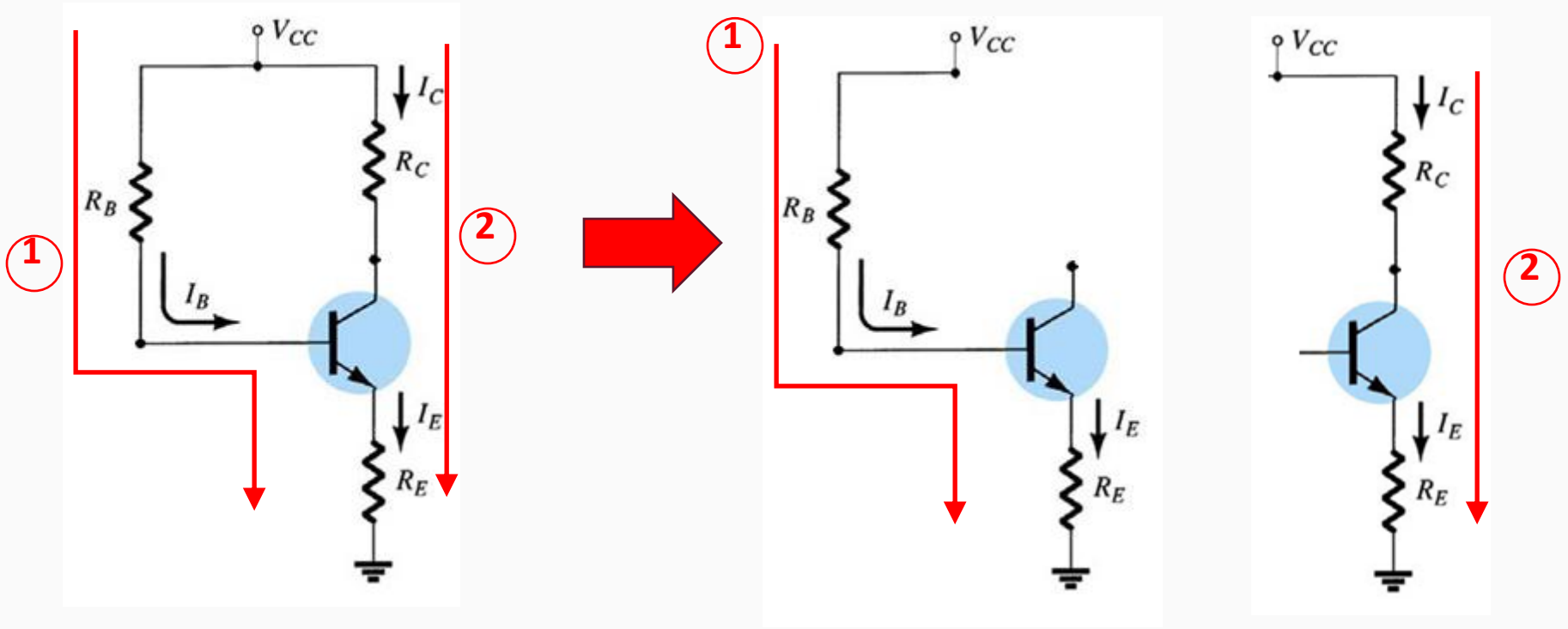
- An emitter resistor, R_E is added to improve stability
- Solve the circuit using HVK
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop
  - CE loop

1st step: Locate capacitors and replace them with an open circuit

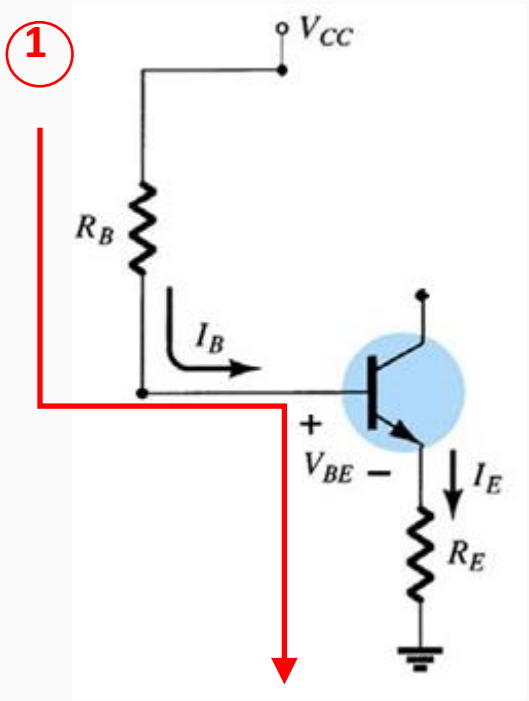


2nd step: Locate 2 main loops

Fixed Base Bias with Emitter Resister



BE Loop Analysis



- From HVK;

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

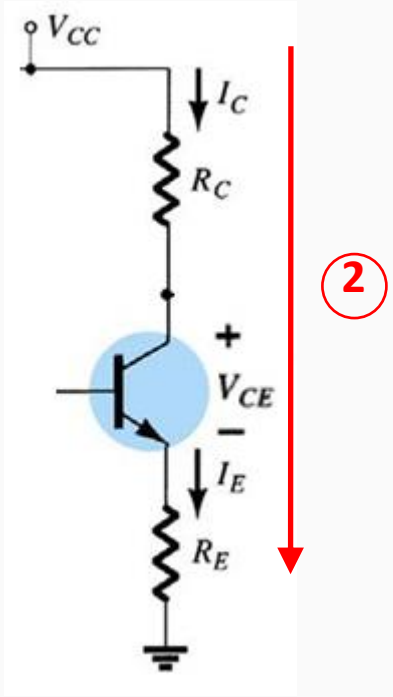
Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

CE Loop Analysis



- From HVK;

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

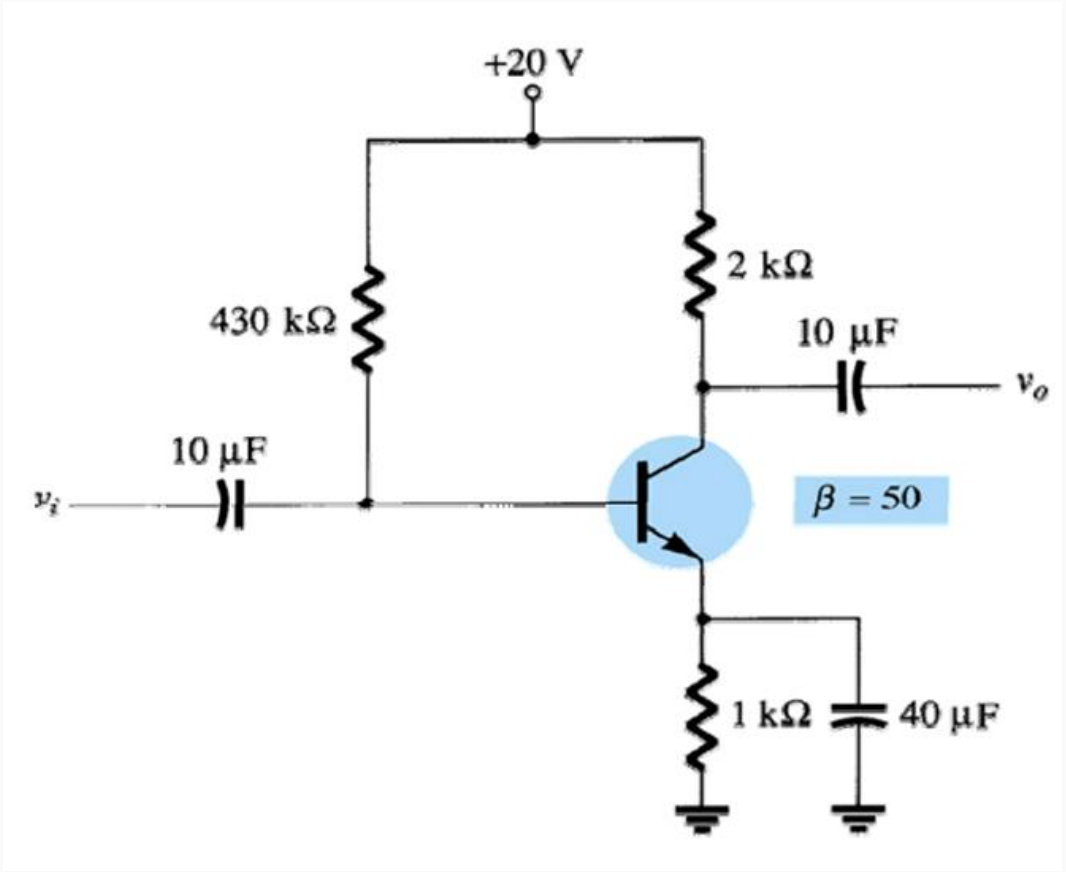
- Assume;

$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Example Emitter Stabilized Bias



- Find I_{CQ}, I_{BQ}, V_{CEQ}, V_{BQ}, V_{CQ}, V_{EQ} & V_{BCQ}? (Silicon transistor);

- Answers;

  I_{CQ} = 2.01 mA

  I_{BQ} = 40.1 μA

  V_{CEQ} = 13.97V

  V_{BQ} = 2.71V

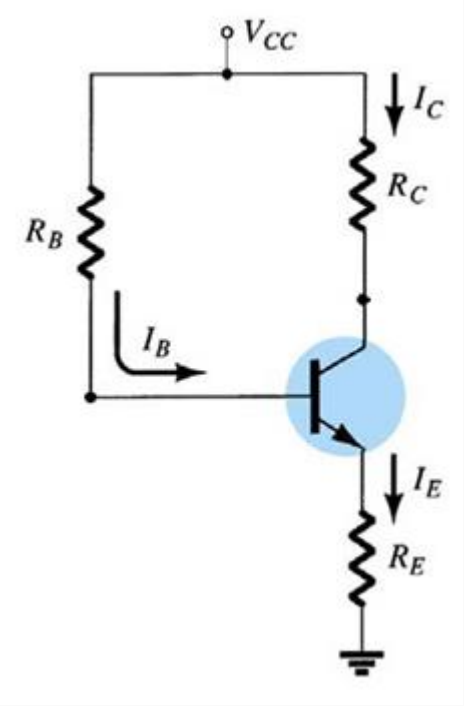
  V_{EQ} = 2.01V

  V_{CQ} = 15.98V

  V_{BCQ} = -13.27V

step 1 : open all capacitors and redraw the circuit.

step 2 :



B - E Loop KVL

$$20 - I_B R_B - V_{BE} - I_E R_E = 0$$

using relation $I_E = (1+\beta) I_B$

$$20 - I_B R_B - V_{BE} - R_E (1+\beta) I_B = 0$$ √

$$I_B = \frac{20 - V_{BE}}{R_B + R_E(1+\beta)} = \frac{20 - 0.7}{430\text{k} + 1\text{k}(1+50)} = \underline{40.1\,\mu\text{A}}$$

using relation $I_E = (1+\beta) I_B$ and $I_E \approx I_C$ √

$$I_E \approx I_C = (1+50) \times 40.1\,\mu = \underline{2.05\,\text{mA}}$$

step 3

C - E Loop KVL

$$20 - I_C R_C - I_E R_E V_{CE} = 0$$

$$V_{CE} = 20 - I_C R_C - I_E R_E$$ √

$$= 20 - (2.05\,\text{m} \times 2\text{k}) - (2.05\,\text{m} \times 1\text{k}) = \underline{13.85\text{V}}$$

it is known that $V_{BE} = 0.7V$

and $V_{BE} = V_B - V_E$ and $V_E = I_E R_E$

$$\therefore V_E = I_E R_E = 2.05m \times 1k = \underline{2.05\ V}$$

$$\therefore V_B = V_{BE} + V_E = 0.7 + 2.05 = \underline{2.75\ V}$$

from $V_{CE} = V_C - V_E$

$$\therefore V_C = V_{CE} + V_E = 13.85 + 2.05 = \underline{15.9\ V}$$

$$V_{BC} = V_B - V_C = 2.75 - 15.9 = \underline{-13.15V}$$

this BJT is biased in <u>FORWARD ACTIVE</u>

Load Line Analysis – Emitter (Stabilized Bias) Circuit

- For V_{CE} = 0, the transistor will be in saturation region
- Taking the transistor's saturation equation: $I_{C_{sat}} = \dfrac{V_{CC}}{R_C + R_E}$

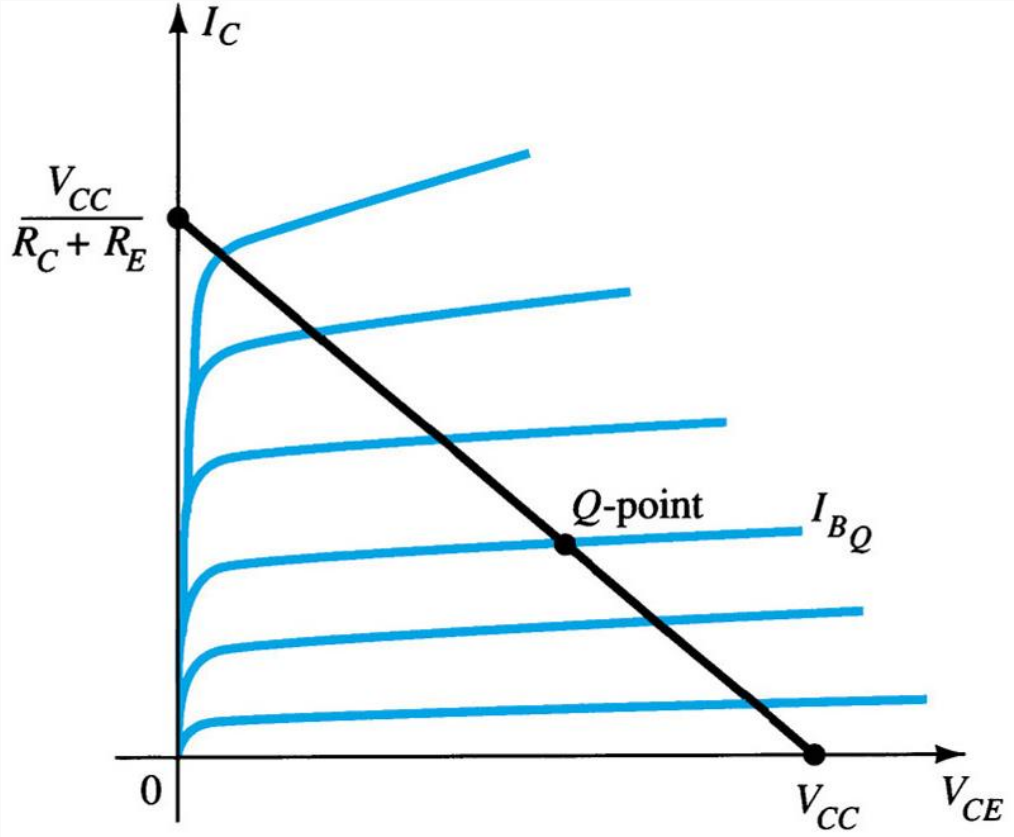
- For I_C = 0: $I_C \approx I_E$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} = 0$$

$$\therefore V_{CE} = V_{CC}$$

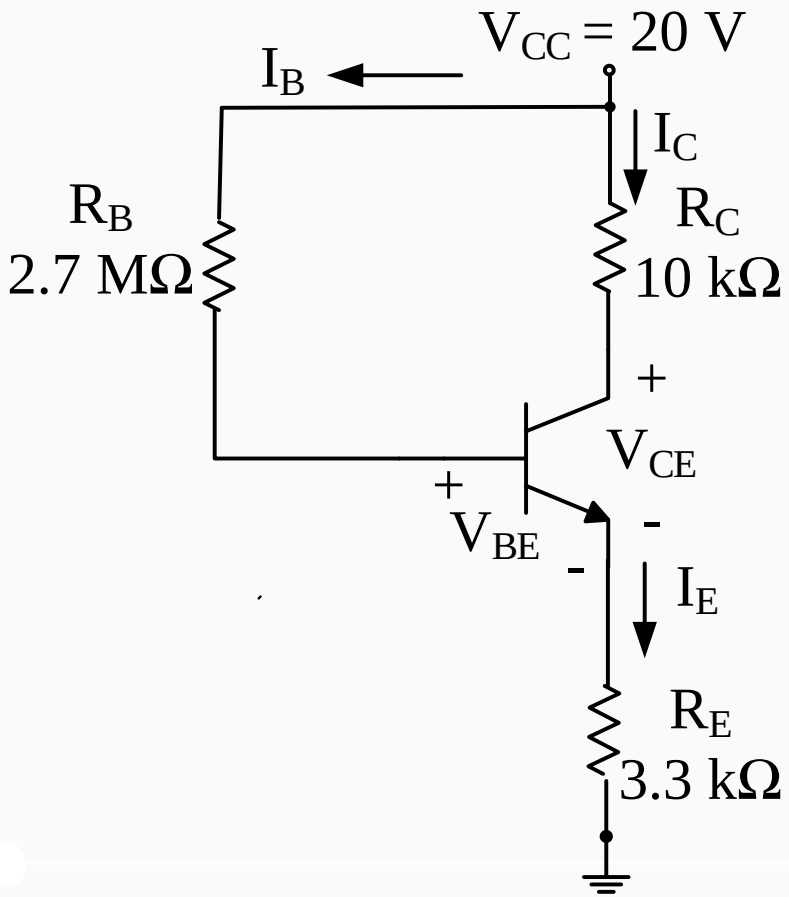
Load Line Analysis – Emitter (Stabilized Bias) Circuit

So, the load-line becomes:



Exercise : Emitter Stabilized Bias

Find I_{CQ}, I_{BQ}, V_{CEQ}, V_{BQ}, V_{CQ}, V_{EQ} & V_{BCQ}? (Silicon transistor). Construct the DC load line and determine the transistor operation region



Exercise Test 2 2013/2014/2

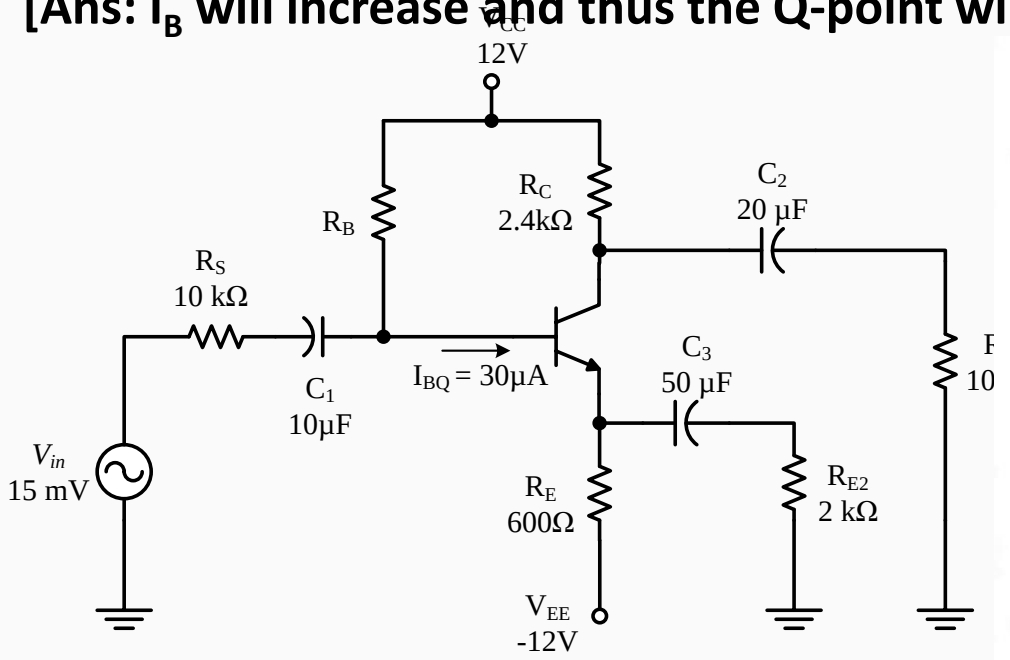
A BJT amplifier circuit in Figure Q2(a) has the following specifications: I_{BQ} = 30μA and V_{BE} = 0.7V.

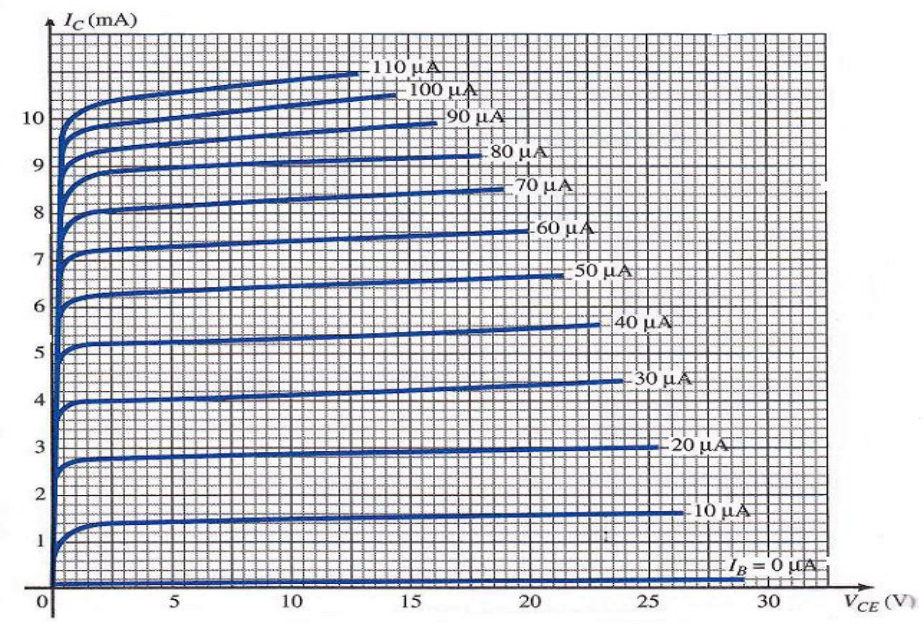
(i) Determine Q-point (I_{CQ}, V_{CEQ}) of the circuit using the output characteristic graph in Figure Q2(b)
[Ans: I_{CQ} = 4.2mA : V_{CEQ} = 11.5V]

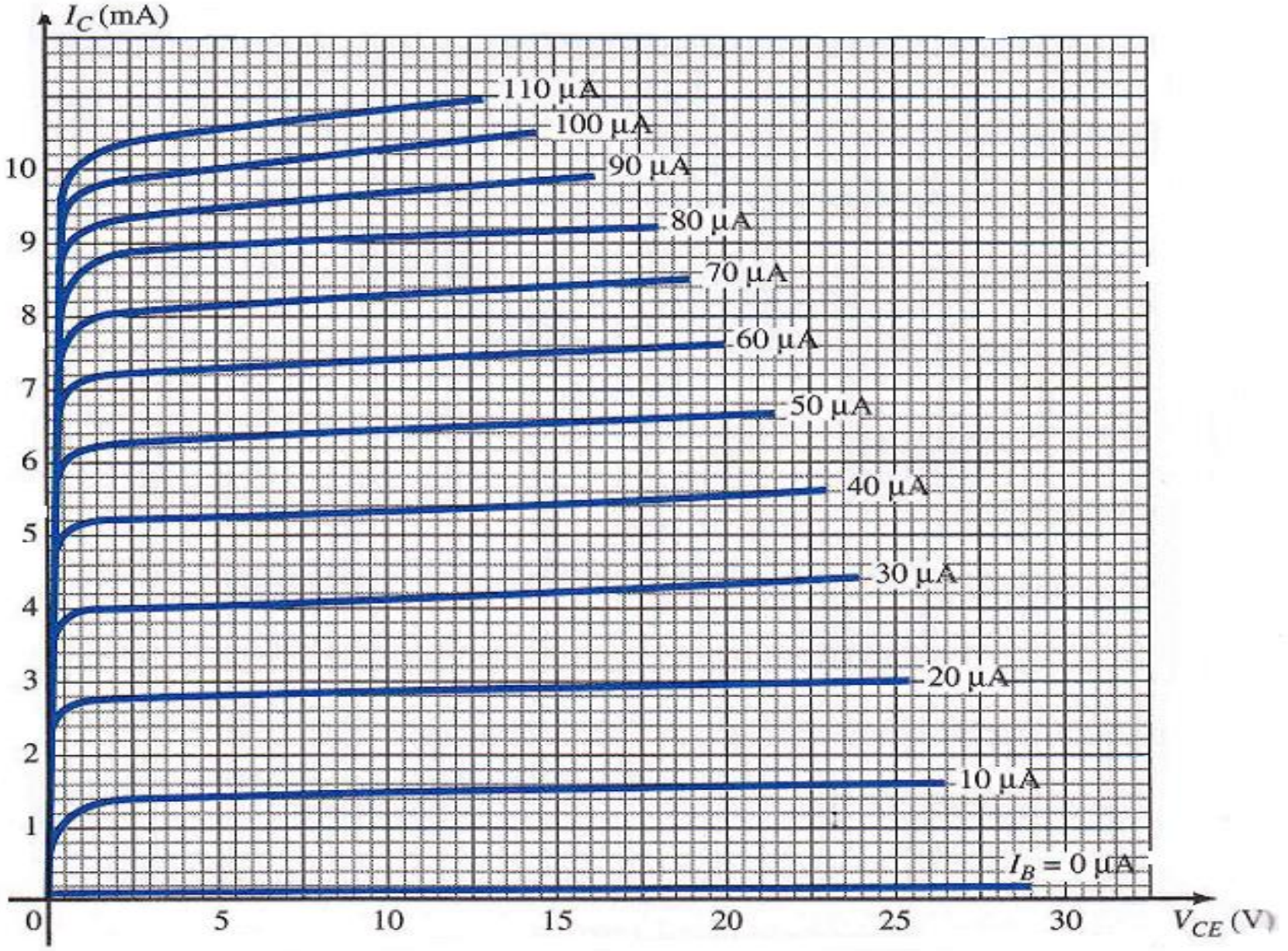
(ii) Calculate β at the Q-point **[Ans: β=140]**

(iii) Calculate R_B **[Ans: 692kΩ]**

(iv) What is the effect on the Q-point of the circuit, when R_B is decreased?
[Ans: I_B will increase and thus the Q-point will move upwards]



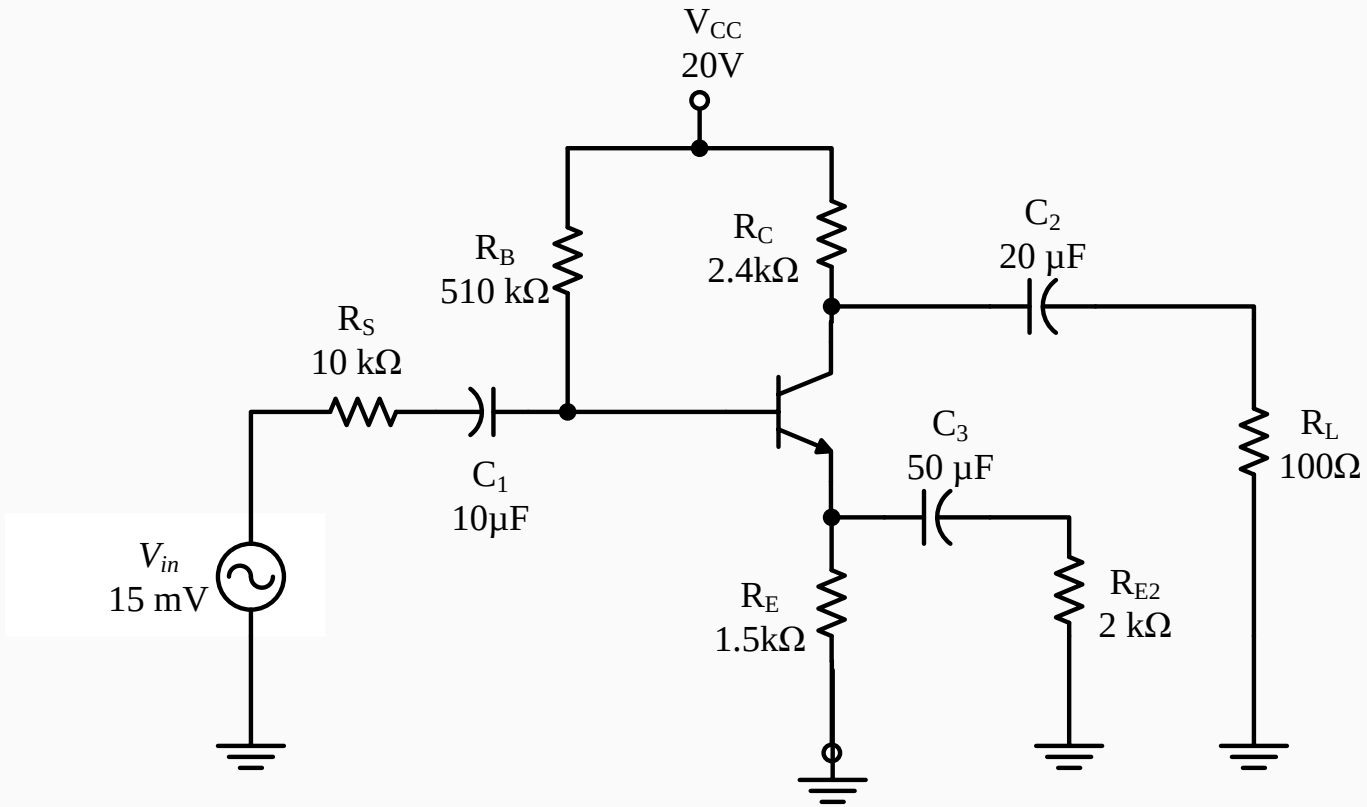



I_C (mA)
110 μA
100 μA
90 μA
80 μA
70 μA
60 μA
50 μA
40 μA
30 μA
20 μA
10 μA
I_B = 0 μA
0
1
2
3
4
5
6
7
8
9
10
5
10
15
20
25
30
V_{CE} (V)

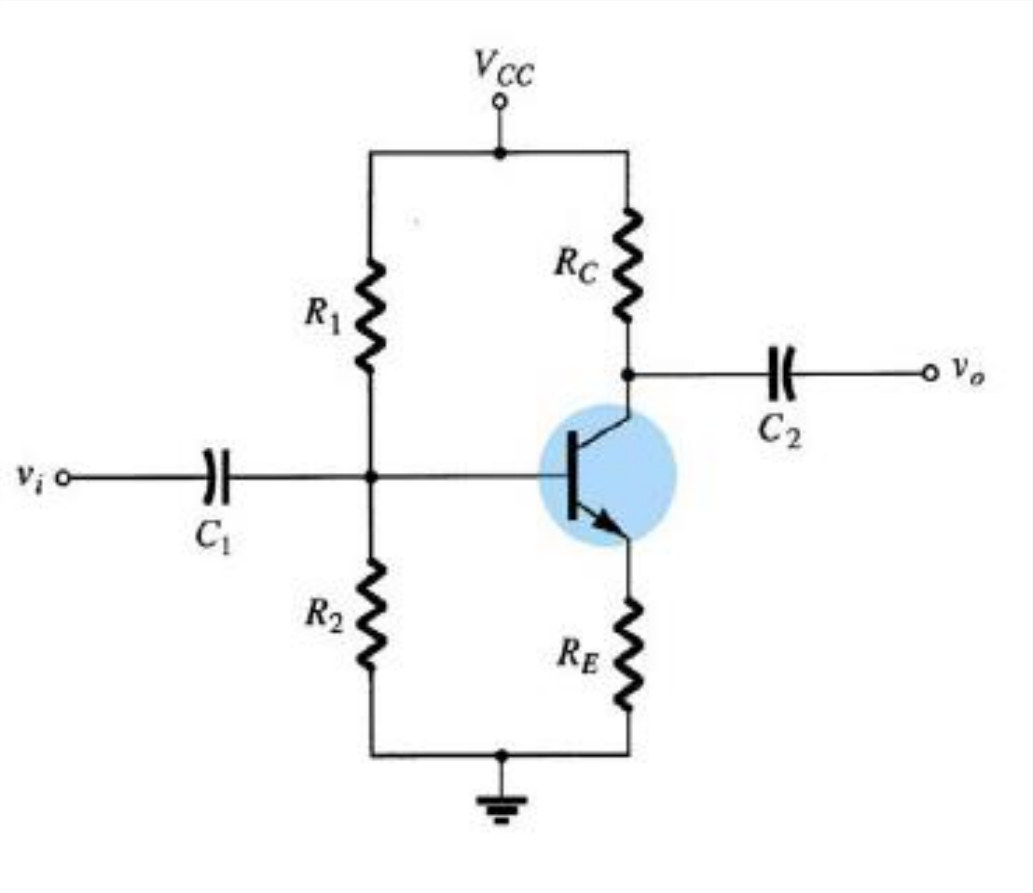
Exercise

Determine I_{BQ}, I_{CQ}, V_{CEQ}, V_B, V_C, V_E. Given β= hFE= 100 and V_{BE}= 0.7V. Sketch the DC load line of the circuit.

[Ans: I_{BQ} =29.18uA, I_{CQ} =2.92 mA, V_{CEQ}=8.61V, V_B=5.12V, V_C=12.99V, V_E = 4.38V]



Voltage Divider Bias Circuit



- Provides good Q-point stability with a single polarity supply voltage
- Solve the circuit using HVK
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Simplified circuit using Thevenin Theorem
- 3rd step: Locate 2 main loops which;
  - BE loop
  - CE loop

Voltage Divider Bias Approximation Analysis

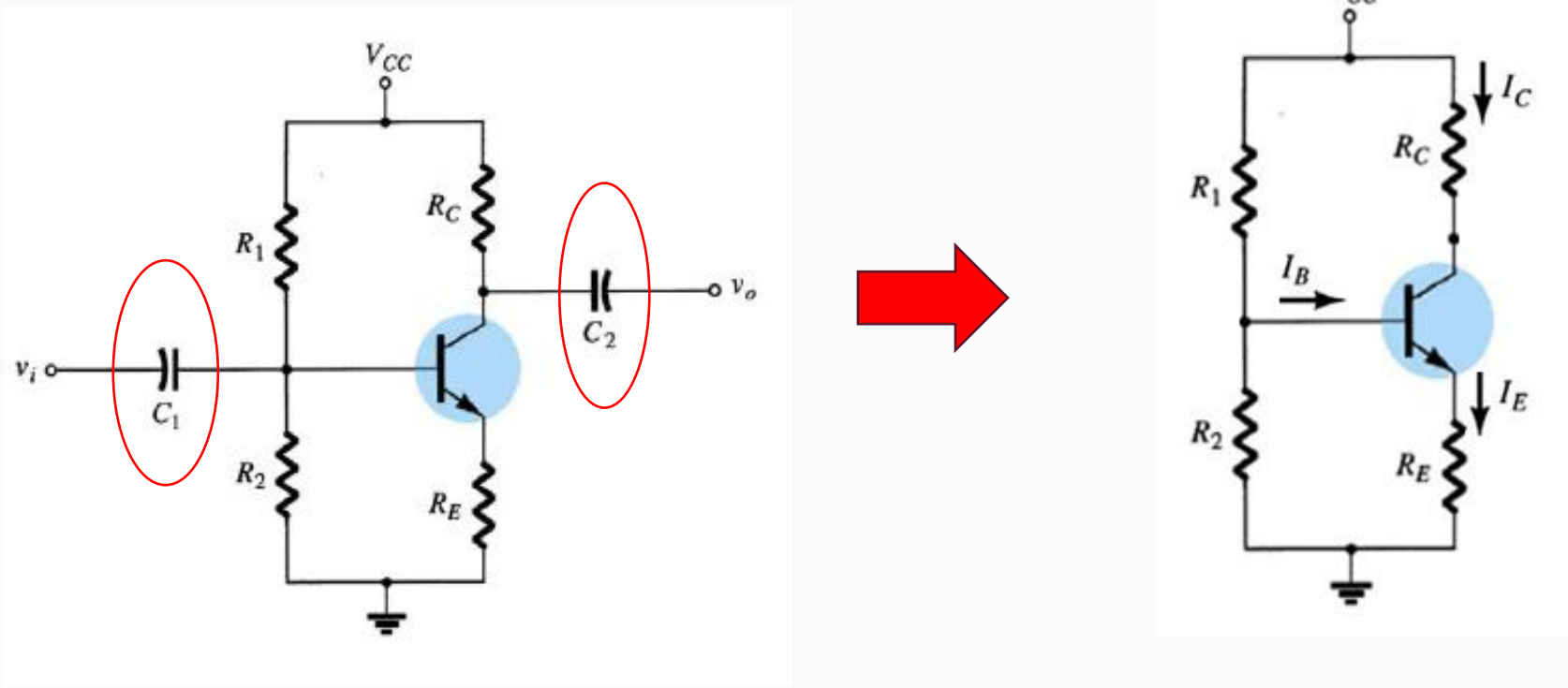
For approximation analysis we can assume

$$V_{TH}=V_B$$

but the following condition must satisfy:

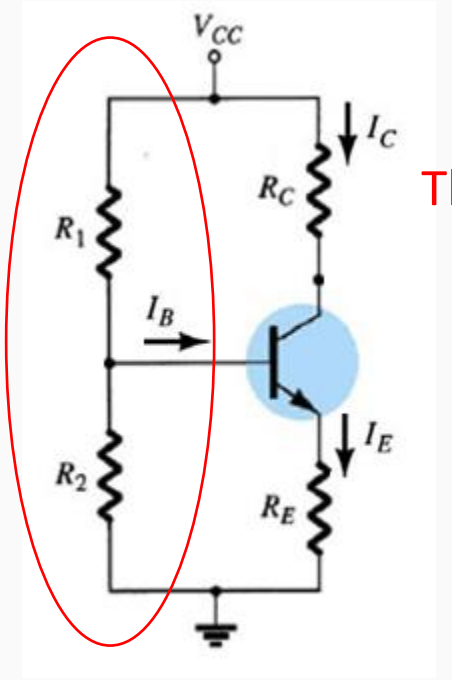
$$\beta R_E \geq 10R_2$$

1st step: Locate capacitors and replace them with an open circuit

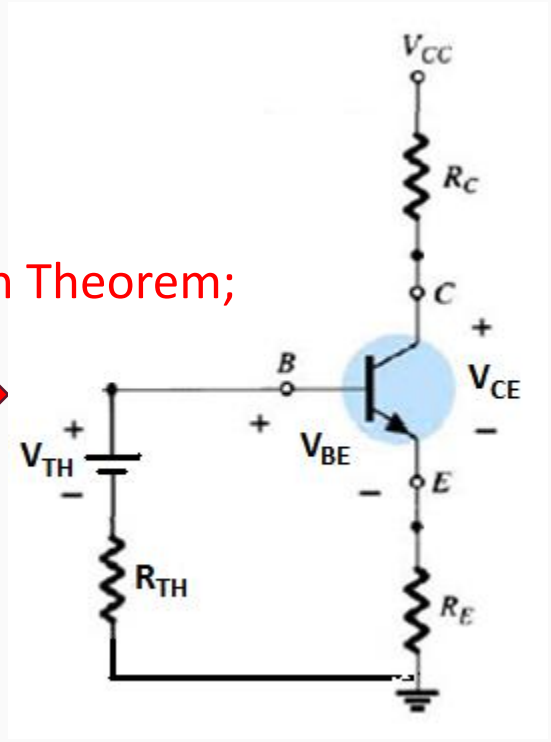


2nd step: : Simplified circuit using Thevenin Theorem

Voltage Divider Bias Circuit



Thevenin Theorem;



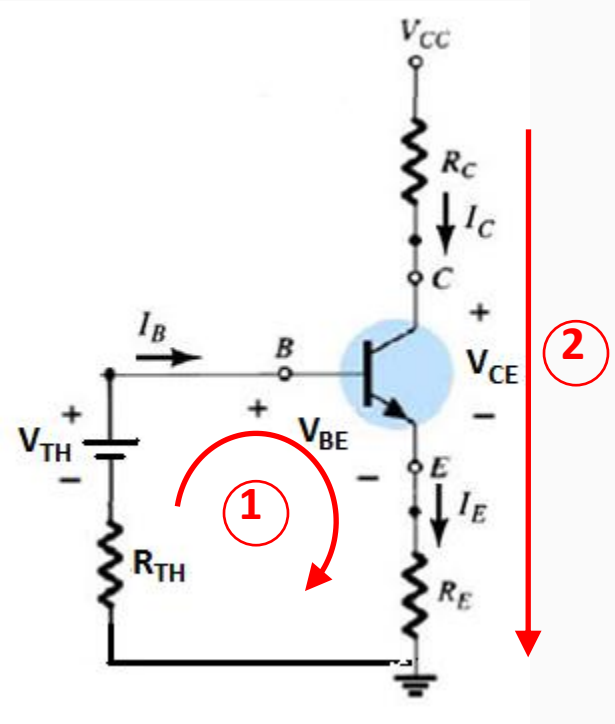
Simplified Circuit

From Thevenin Theorem;

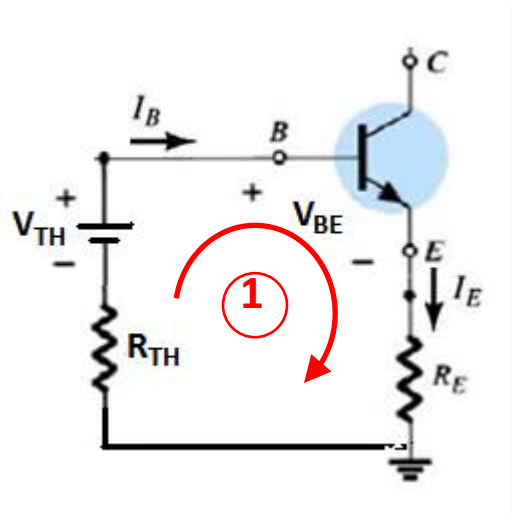
$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

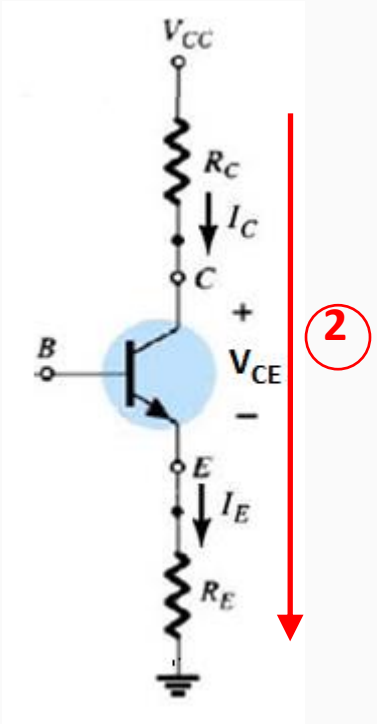
3rd step: Locate 2 main loops



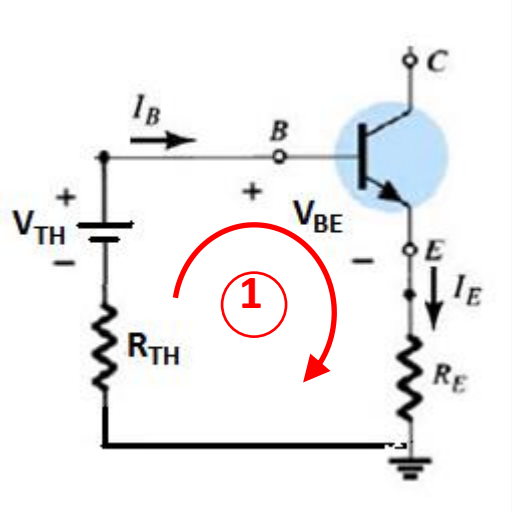
BE Loop



CE Loop



BE Loop Analysis



- From HVK;

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

Recall; $I_E = (\beta + 1) I_B$

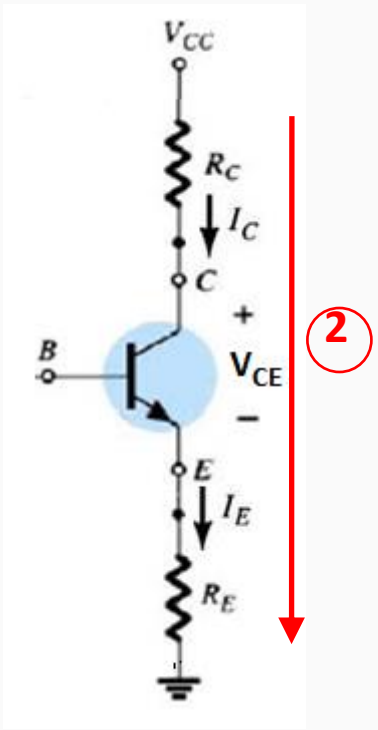
Subtitute for I_E

$$V_{TH} - I_B R_{TH} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{RTH} + (\beta + 1) R_E}$$

CE Loop Analysis

Voltage Divider Bias Circuit



- From HVK;

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

- Assume;

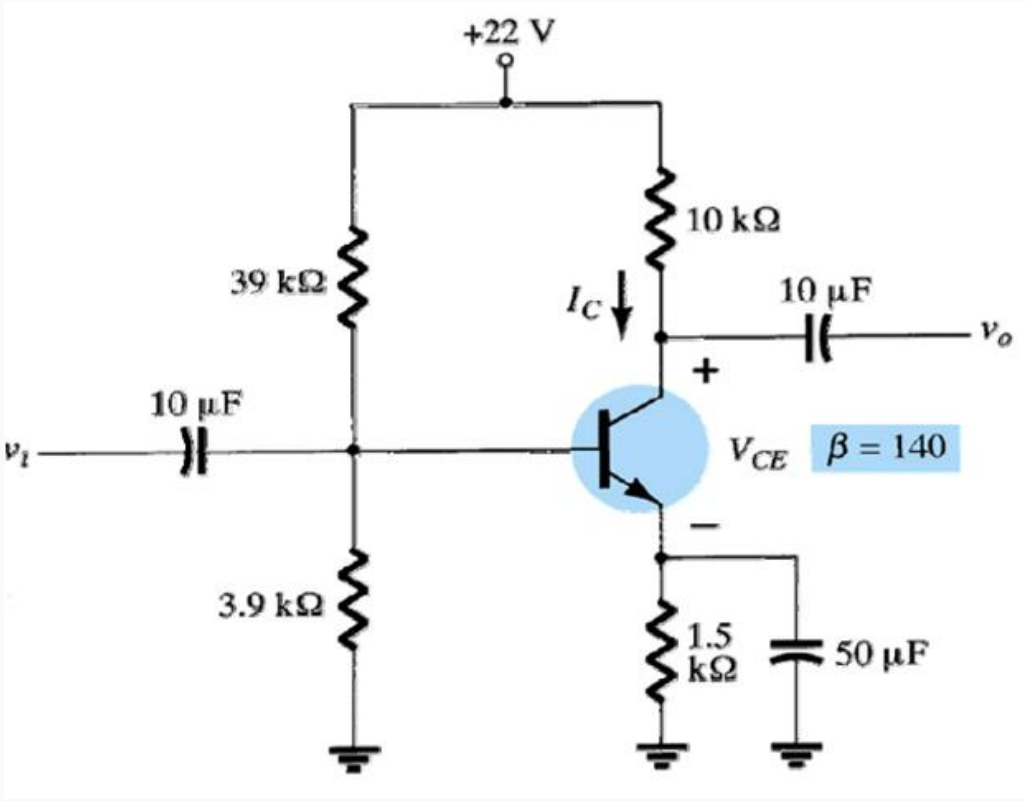
$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Example Voltage Divider Bias Circuit: Single Supply

- Find R_{TH}, V_{TH}, I_{CQ}, I_{BQ}, V_{CEQ}, V_{BQ}, V_{CQ}, V_{EQ} & V_{BCQ}? (Silicon transistor). Construct the DC load line



- Answers;

  RTH = 3.55 kΩ

  VTH = 2V

  ICQ = 0.85 mA

  IBQ = 6.05 μA

  VCEQ = 12.9V

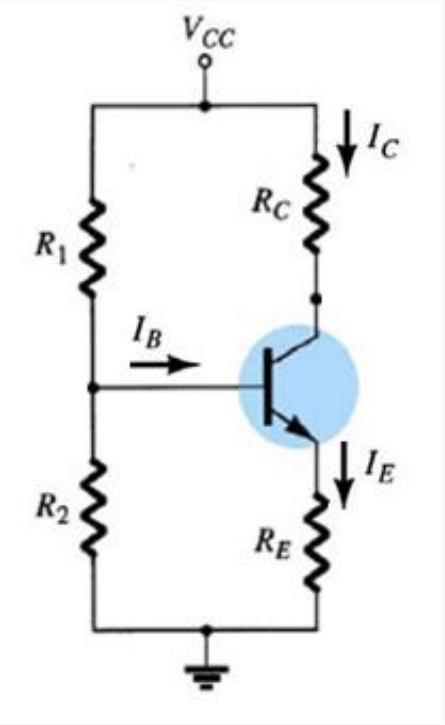
  VBQ = 1.978V

  VEQ = 1.275V

  VCQ = 13.5V

  VBC = -12.81V

step 1 : open all capacitors and redraw the circuit.

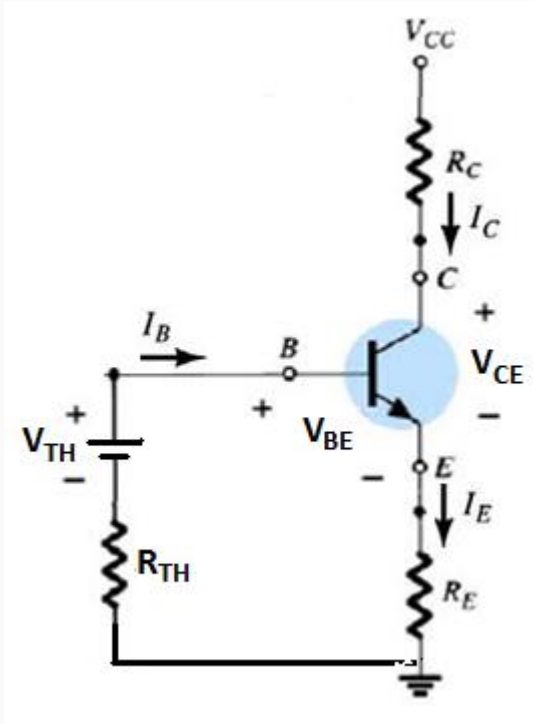


step 2 : calculate V_{th} and R_{th}

$$V_{th} = \frac{3.9k}{3.9k + 39k} \times 22 = 2V$$

$$R_{th} = \frac{3.9k \times 39k}{3.9k + 39k} = 3.55\,k\Omega$$

then redraw the circuit.



step 3 :

B - E Loop KVL

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$2 - I_B(3.55\,k) - 0.7 - I_E(1.5k) = 0$$

using relation $I_E = (1+\beta) I_B$

$$2 - I_B(3.55\,k) - 0.7 - I_B(1+\beta)(1.5k) = 0$$

$$I_B = \frac{2 - 0.7}{3.55k + 1.5k(1+140)} = \underline{6.05\,\mu A}$$

using relation $I_E = (1+\beta) I_B$ and $I_E \approx I_C$

$$I_E \approx I_C = (1+140) \times 6.05\,\mu = \underline{0.85\,mA}$$

C - E Loop KVL

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\text{assume } I_C \approx I_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 22 - 10\text{k}(0.85\text{m}) - 1.5\text{k}(0.85\text{m})$$

$$V_{CE} = \underline{12.19\text{V}}$$

it is known that $V_{BE} = 0.7\text{V}$

and $V_{BE} = V_B - V_E$ and $V_E = I_E R_E$

$$\therefore V_E = I_E R_E = 0.85\text{m} \times 1.5\text{k} = \underline{1.28\text{ V}}$$

$$\therefore V_B = V_{BE} + V_E = 0.7 + 1.28 = \underline{1.98\text{ V}} \approx V_{TH}$$

from $V_{CE} = V_C - V_E$

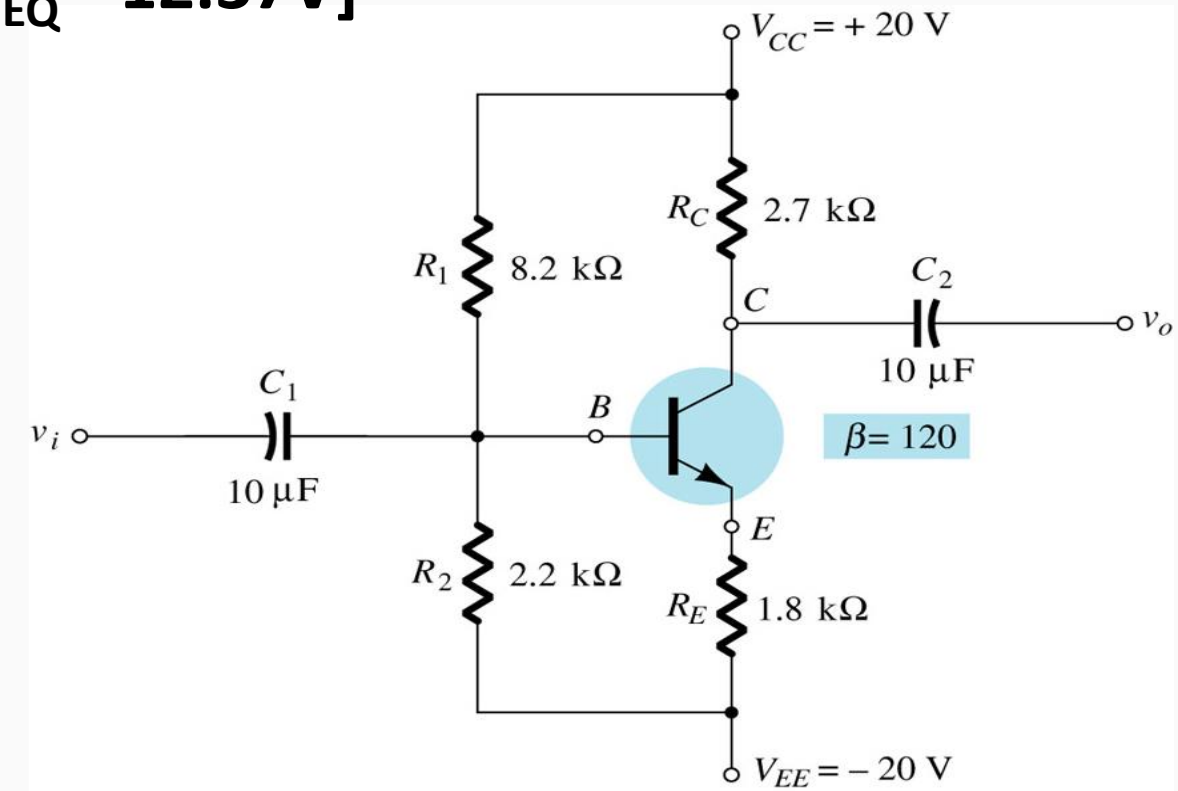
$$\therefore V_C = V_{CE} + V_E = 12.19 + 1.28 = \underline{13.51\text{ V}}$$

$$V_{BC} = V_B - V_C = 0.7 - 13.51 = \underline{-12.81\text{V}}$$

this BJT is biased in <u>FORWARD ACTIVE</u>

Example Voltage Divider Bias with 2 supply

Determine I_{BQ}, I_{CQ}, V_{CEQ}, V_{BQ}, V_{CQ}, V_{EQ}. Given $\beta = h_{FE} = 120$ and $V_{BE} = 0.7V$.
[Ans: I_{BQ} = 35.35µA, I_{CQ} = 4.24 mA, V_{CEQ} = 20.92 V, V_{BQ} = –11.6 V, V_{CQ}=8.55V, V_{EQ}=-12.37V]



Solution

step 1 : open all capacitors and draw the DC equivalent circuit

step 2 : calculate V_{th} and R_{th}

$$V_{th} = \frac{R_2}{R_1 + R_2} \times (+V_{CC}) + \frac{R_1}{R_1 + R_2} \times (-V_{CC})$$

$$V_{th} = \frac{2.2k}{2.2k + 8.2k} \times (+20) + \frac{8.2k}{2.2k + 8.2k} \times (-20) = \underline{-11.54V}$$

$$R_{th} = \frac{2.2k \times 8.2k}{2.2k + 8.2k} = 1.73k\Omega$$

step 3 :

B - E Loop KVL

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E + V_{EE} = 0$$

using relation $I_E = (1+\beta) I_B$

$$V_{TH} - I_B R_{TH} - V_{BE} - (1+\beta) I_B R_E + V_{EE} = 0$$

$$-11.54 - I_B(1.73k) - 0.7 - (1+120) I_B(1.8k) + 20 = 0$$

$$I_B = I_{BQ} = \frac{20 - 11.54 - 0.7}{1.73\,k + 1.8k(1+120)} = \underline{35.35\,\mu A}$$

using relation $I_E = (1+\beta) I_B$ and $I_E \approx I_C$

$$I_E \approx I_C \approx I_{CQ} = (1+120) \times 35.35\,\mu = \underline{4.28\,mA}$$

C - E Loop KVL

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

assume $I_C \approx I_E$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E + V_{EE} = 20 - 2.7\text{k}(4.28\text{m}) - 1.8\text{k}(4.28\text{m}) + 20$$

$$V_{CE} = \underline{V_{CEQ} = 20.74\text{V}}$$

It is known that $V_{BE} = 0.7\text{V}$

and $V_{BE} = V_B - V_E$ and $V_E = I_E R_E - V_{EE}$

$$\therefore V_E = I_E R_E - V_{EE} = 1.8\text{k}(4.28\text{m}) - 20 = \underline{-12.3\ \text{V}}$$

$$\therefore V_B = V_{BE} + V_E = 0.7 - 12.3 = \underline{-11.6\text{V}} \approx V_{TH}$$

from $V_{CE} = V_C - V_E$

$$\therefore V_C = V_{CE} + V_E = 20.74 - 12.3 = \underline{8.44\ \text{V}}$$

Exercise FINAL SEU 2012 2010/2011/2

Refer to a small signal amplifier circuit in Figure Q3. The transistor's parameter are:

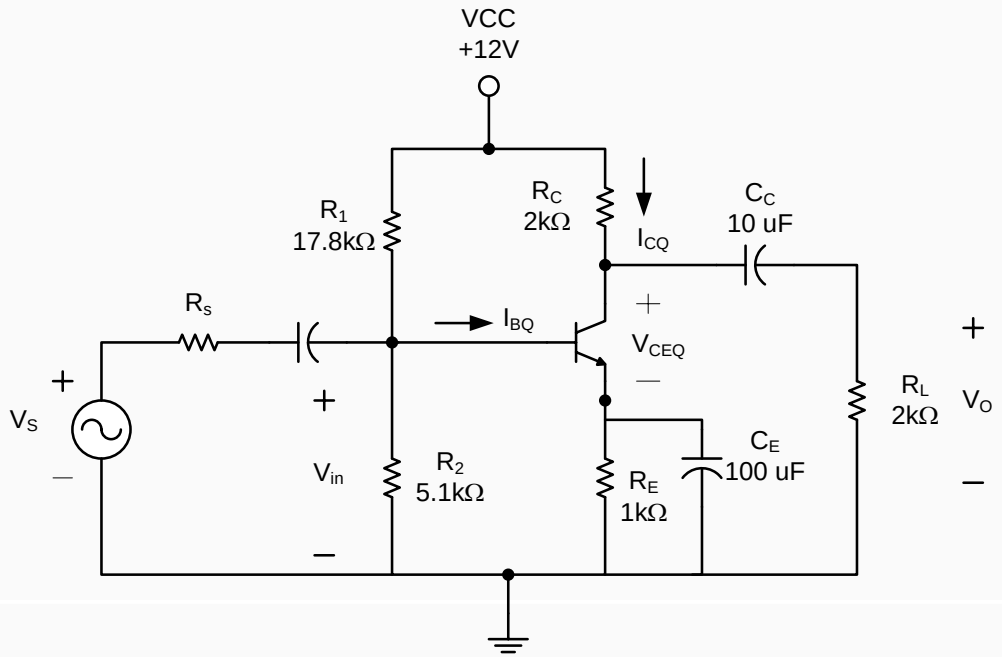
$\beta_{DC} = \beta_{AC} = 100$, $V_{BE} = 0.7V$, $V_T = 26mV$

I. Draw the DC equivalent circuit.

II. Calculate the base and collector current, I_{BQ} and I_{CQ}. **[Ans: I_{BQ}=18.7µA, I_{CQ}=1.87mA]**

III. Calculate the collector to emitter voltage, V_{CEQ}. **[Ans=V_{CE}=6.3V]**

IV. Calculate new Q-point (I_{BQ} and I_{CQ}) if R_2 is halved **[Ans: I_B=7.7µA, I_C=0.77mA]**



Load Line Analysis - Voltage Divider Bias

- For the load-line analysis, the cutoff region still results the same as the fixed bias and emitter bias configuration:

$$V_{CE} = V_{CC}\Big|_{I_C=0}$$

- And for the saturation region:

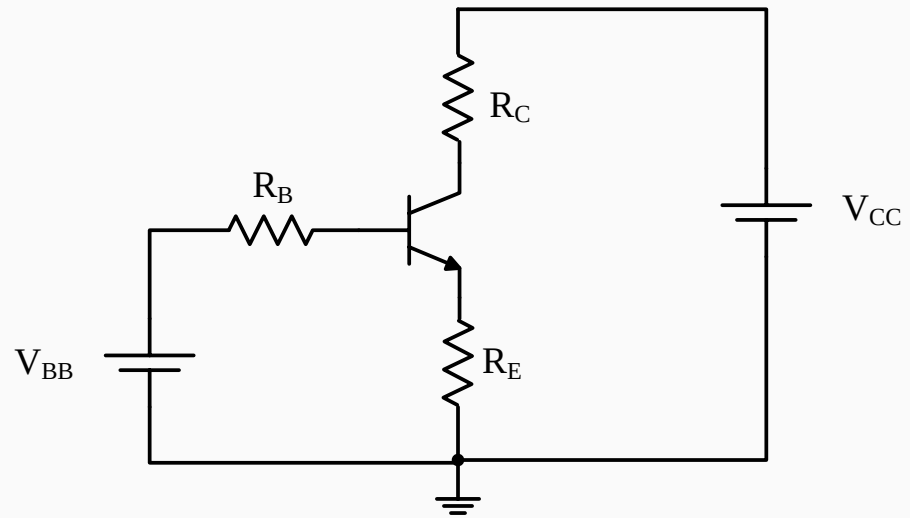
$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}\Bigg|_{V_{CE}=0}$$

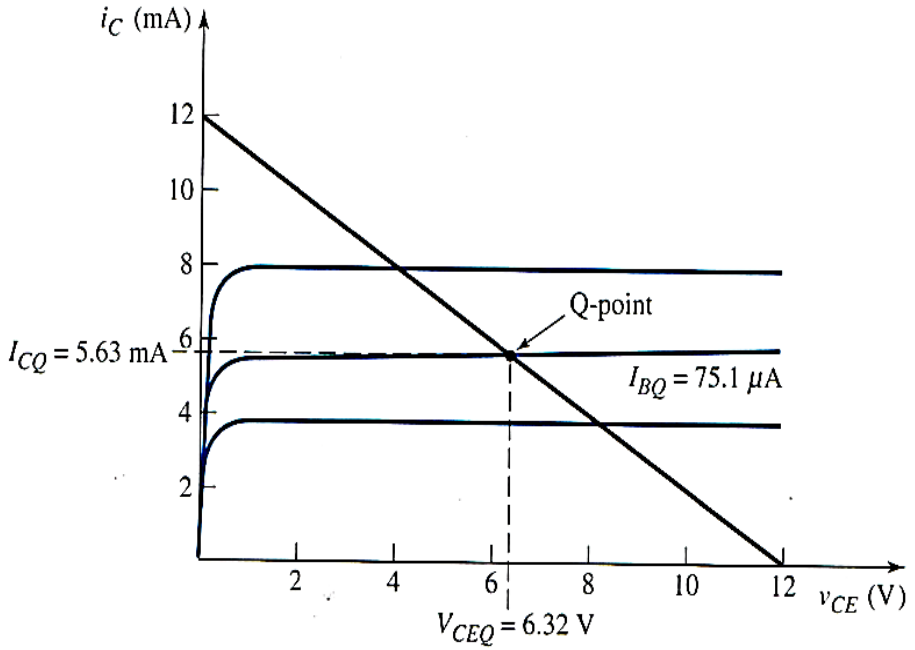
Exercise Final Exam 2013/2014/2

The dc load line of the circuit and the characteristic is as shown. Based on the figures,

(i) Determine the common emitter current gain, β, and the emitter current, I_E.
[Ans: β = 75, I_E= 5.71mA]

(ii) Determine R_B and R_C such that the circuit yields the given Q-point. Given V_{BE} = 0.7 V, V_{BB} = 6 V, and R_E = 600 Ω. **[Ans: R_B=25kΩ, R_C=400Ω]**





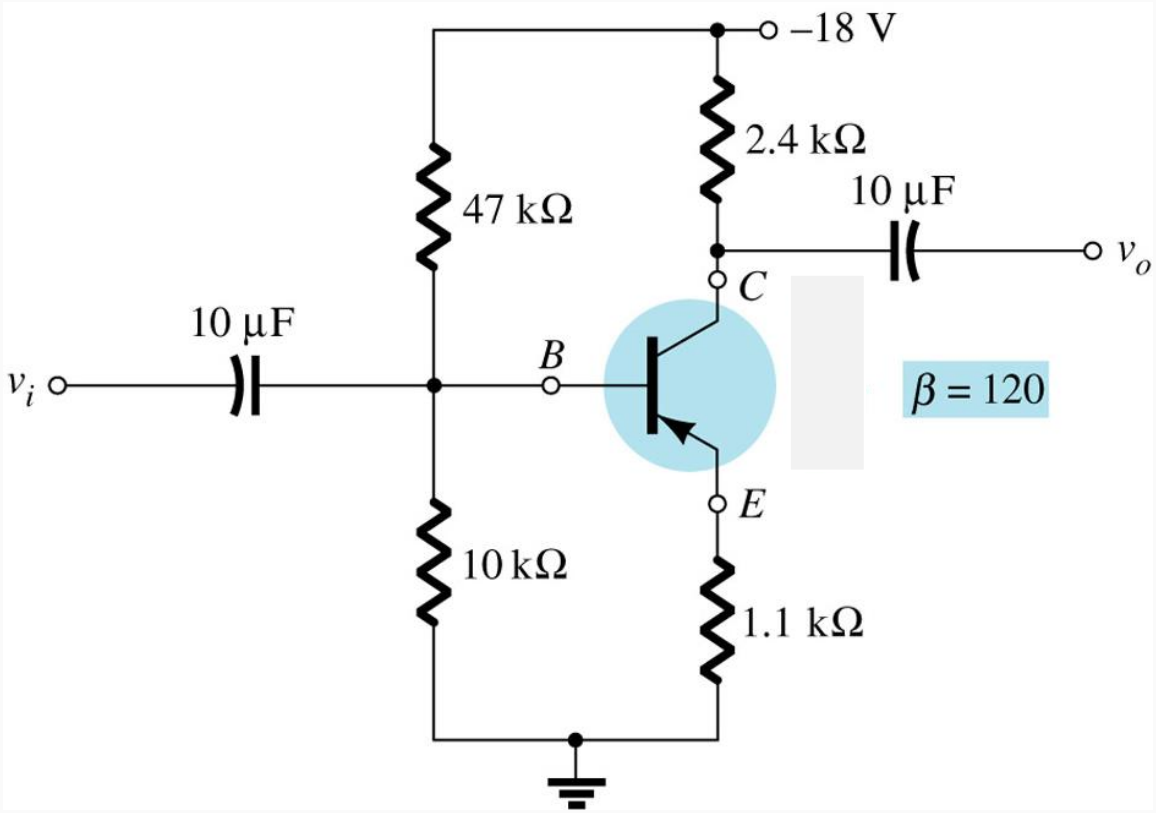
DC Biasing Circuit for PNP BJT

- All the previous analysis and technique used in NPN BJT can be applied to PNP BJT.
- This is because the amount of current is the same; $I_E=I_B+I_C$
- The major different is the direction of current flowing.
- PNP BJT current flow from emitter to collector.

Example Voltage Divider PNP

Determine I_{BQ}, I_{CQ}, V_{CEQ},V_B,V_C and V_E. Given β = 120 and V_{EB} = 0.7.

[Ans: I_{BQ} =17.4uA, I_{CQ}=2.09 mA ,V_{CEQ}=-10.68, V_B =-3V, V_C =-12.98V and V_E = -2.32V]



Solution

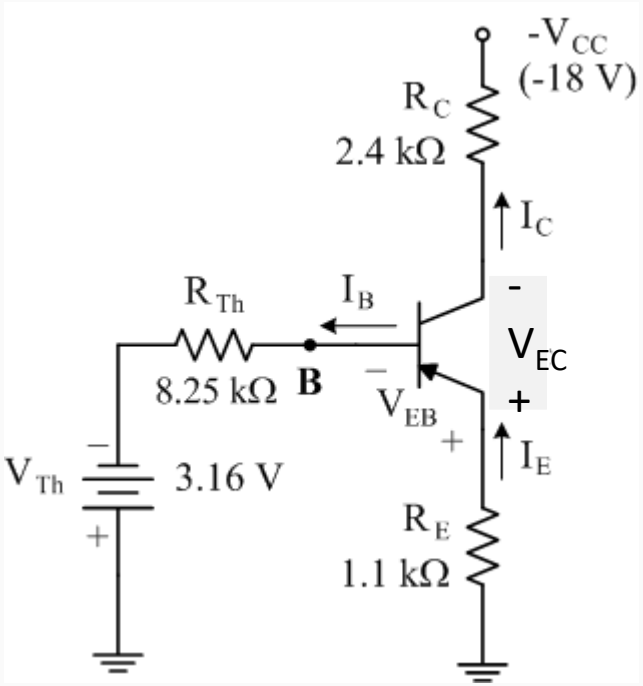
step 1 : open all capacitors and draw the DC equivalent circuit.

step 2 : calculate V_{th} and R_{th}

$$V_{th} = \frac{10k}{10k + 47k} \times -18 = -3.16V$$

$$R_{th} = \frac{10k \times 47k}{10k + 47k} = 8.25\,k\Omega$$

then redraw the circuit.



step 3 :

E - B Loop KVL

$$I_E R_E - V_{EB} V_{TH} - I_B R_{TH} + V_{TH} = 0$$

using relation $I_E = (1+\beta) I_B$

$$I_B (1+\beta) R_E - V_{EB} - I_B R_{TH} + V_{TH} = 0$$

$$I_B (1+120)(1.1k) - 0.7 - I_B (8.25\,k) + 3.16 = 0$$

$$I_B = I_{BQ} = \frac{3.16 - 0.7}{8.25\,k + 1.1k(1+120)} = \underline{17.4\,\mu A}$$

using relation $I_E = (1+\beta) I_B$ and $I_E \approx I_C$

$$I_E \approx I_C \approx I_{CQ} = (1+120) \times 17.4\,\mu = \underline{2.09\,mA}$$

E - C Loop KVL

$$-I_E R_E - V_{EC} - I_C R_C + V_{CC} = 0$$

assume $I_C \approx I_E$

$$V_{EC} = I_E R_E - I_C R_C + V_{CC} = -1.1\text{k}(2.09\text{m}) - 2.4\text{k}(2.09\text{m}) + 18$$

$$V_{EC} = V_{ECQ} = \underline{10.69\text{V}} \qquad \therefore V_{CE} = V_{CEQ} = \underline{-10.69\text{V}}$$

it is known that $V_{EB} = 0.7\text{V}$

and $V_{EB} = V_E - V_B$ and $V_E = -I_E R_E$

$$\therefore V_E = -I_E R_E = -2.09\text{m} \times 1.1\text{k} = \underline{-2.3\,\text{V}}$$

$$\therefore V_B = V_E - V_{EB} = -2.3 - 0.7 = \underline{-3\,\text{V}}$$

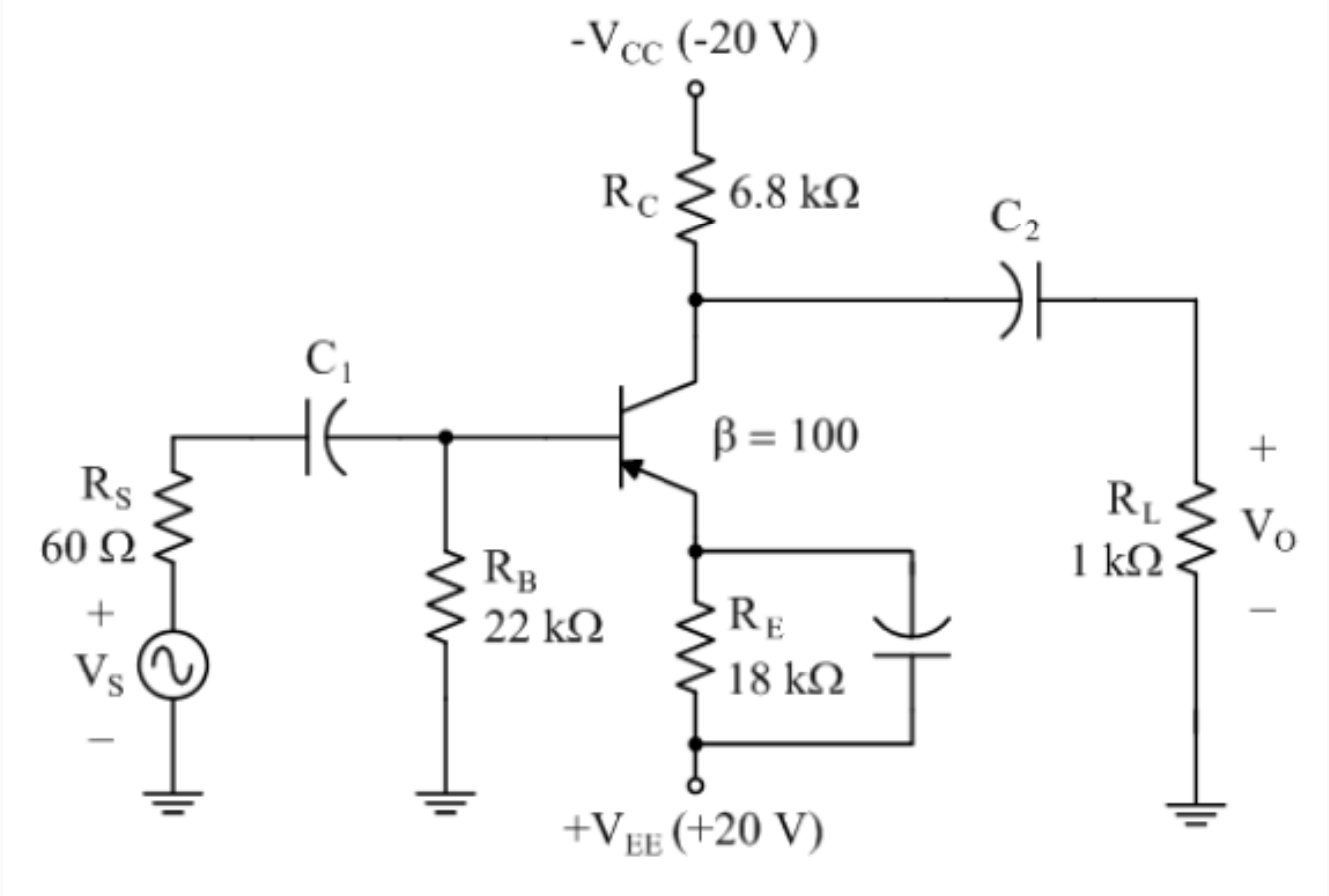
from $V_{EC} = V_E - V_C$

$$\therefore V_C = V_E - V_{EC} = -2.3 - 10.69 = \underline{-12.99\,\text{V}}$$

Example Fixed Bias with 2 supply

Determine I_{BQ}, I_{CQ}, V_{CEQ}, V_B, V_C, V_E. Given $\beta = h_{FE} = 100$ and $V_{EB} = 0.7V$.

[Ans: I_{BQ}=10.49uA, I_{CQ}=1.05mA, V_{CEQ}=-13.96V, V_B=0.2V V_C=-12.86V and V_E =0.93V]



Solution

step 1 : open all capacitors and draw the DC equivalent circuit.

step 2 :

E - B Loop KVL

$$20 - I_E R_E - V_{EB} - I_B R_B = 0$$

using relation $I_E = (1+\beta) I_B$

$$20 - (1+\beta) I_B R_E - V_{EB} - I_B R_B = 0$$

$$I_B = \frac{20 - V_{EB}}{R_B + R_E(1+\beta)} = \frac{20 - 0.7}{22k + 18k(1+100)} = \underline{10.49\,\mu A}$$

using relation $I_E \approx I_C$

$$I_E \approx I_C = (1+100) \times 10.49\,\mu = \underline{1.06\,mA}$$

step 3

E - C Loop KVL

$$V_{EE} - I_E R_E - V_{EC} - I_C R_C + V_{CC} = 0$$

$$20 - 18k(1.06) - V_{EC} - 6.8k(1.06) + 20 = 0$$

$$V_{EC} = 20 - 18k(1.06) - 6.8k(1.06) + 20$$

$$V_{EC} = V_{ECQ} = \underline{13.73V}$$

$$\therefore V_{CE} = V_{CEQ} = \underline{-13.73V}$$

We know $\Rightarrow V_{EB} = V_E - V_B$ and $V_E = -I_E R_E + V_{EE}$

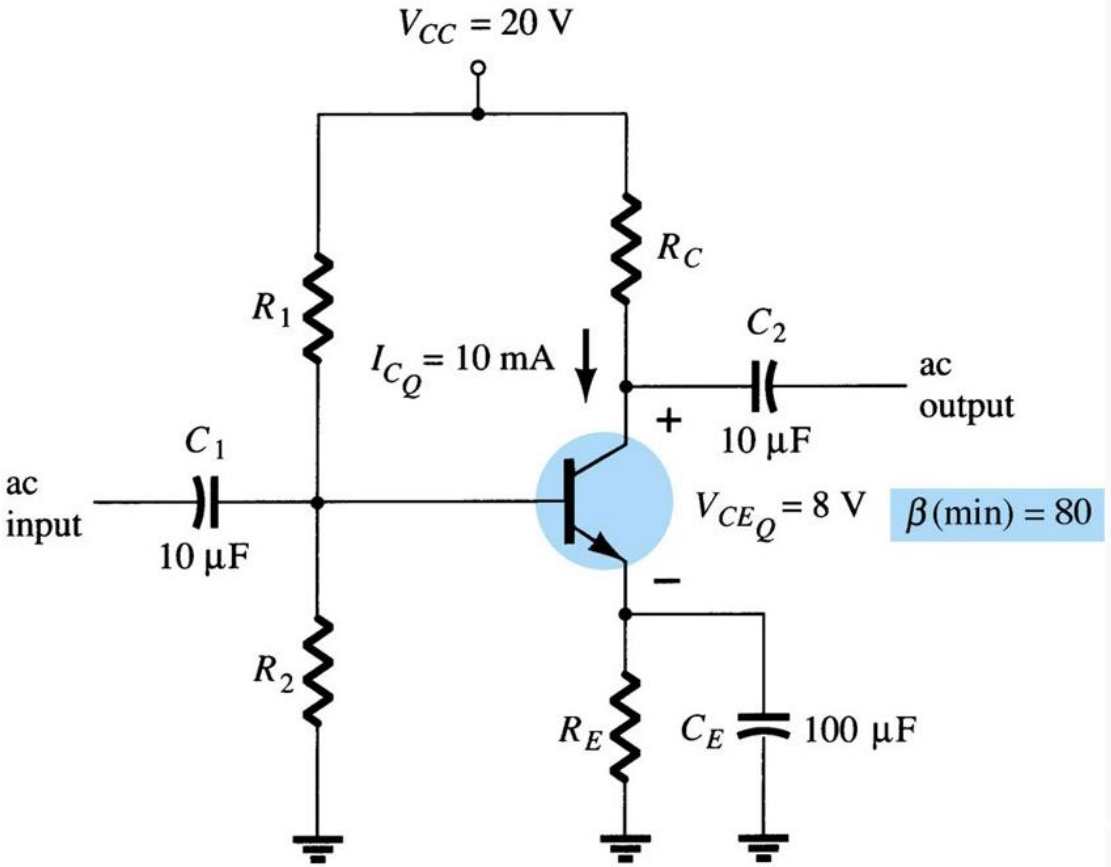
Therefore $V_E = -I_E R_E + V_{EE} = (-1.06m)18k + 20 = \underline{0.92V}$

$$\therefore V_B = V_E - V_{EB} = 0.92 - 0.7 = \underline{0.22V}$$

$$\text{and } V_C = V_E - V_{EC} = 0.92 - 13.73 = \underline{-12.81V}$$

Exercise : Design

Determine all the resistors R_E, R_C, R_2 and R_1 values in designing the fixed bias with emitter-stabilized circuit as below. Given $\beta_{min} = h_{FE(min)} = 80$ and $V_{BE} = 0.7$ V, $V_{CEQ} = 8$ V and $I_{CQ} = 10$ mA. Assume $V_E = (1/10)V_{CC}$ and $\beta R_E = 10R_2$. [Ans: $R_E = 197.53\Omega$, $RC = 1k\Omega$, $R_1 = 10.12\ k\Omega$, $R_2 = 1.58k\Omega$]



Exercise

Calculate the value for R_C, R_B, V_{CE} and β for a fixed bias circuit if V_{CC}= 24V, I_B = 20µA dan I_C = 3mA. Transistor must properly biased to achieve maximum symmetrical output swing for the voltage and current. Given V_{BE} = 0.7V.

Example
Transistor Specification & Data Sheet

Answer the following questions by referring to the partial transistor data sheet for transistor 2N3904.

a) What is the maximum collector to emitter voltage?

b) How much continuous collector current can the 2N3904 handle?

c) How much power can 2N3904 dissipate if the ambient temperature is 25° C?

d) What is the minimum and maximum β?

Data Sheet for BJT

Absolute Maximum Ratings(1), (2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C

Notes:

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

Thermal Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Maximum			Unit
		2N3904	MMBT3904(3)	PZT3904(4)	
P_D	Total Device Dissipation	625	350	1,000	mW
	Derate Above 25°C	5.0	2.8	8.0	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

Notes:

3. Device is mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.
4. Device is mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm, mounting pad for the collector lead minimum 6 cm^2.

Data Sheet for BJT

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	6.0		V
I_{BL}	Base Cut-Off Current	V_{CE} = 30 V, V_{EB} = 3 V		50	nA
I_{CEX}	Collector Cut-Off Current	V_{CE} = 30 V, V_{EB} = 3 V		50	nA
ON CHARACTERISTICS(5)					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V	40		
		I_C = 1.0 mA, V_{CE} = 1.0 V	70		
		I_C = 10 mA, V_{CE} = 1.0 V	100	300	
		I_C = 50 mA, V_{CE} = 1.0 V	60		
		I_C =100 mA, V_{CE} = 1.0V	30		
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA		0.2	V
		I_C = 50 mA, I_B = 5.0 mA		0.3	
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA	0.65	0.85	V
		I_C = 50 mA, I_B = 5.0 mA		0.95	
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	300		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 100 kHz		4.0	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 100 kHz		8.0	pF
NF	Noise Figure	I_C = 100 µA, V_{CE} = 5.0 V, R_S = 1.0 kΩ, f = 10 Hz to 15.7 kHz		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10 mA, I_{B1} = I_{B2} = 1.0 mA		200	ns
t_f	Fall Time			50	ns

Note:

5. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2.0%.