CURRICULUM VITAE

A. PERSONAL DETAILS

Name: Mohd Shahrizal Bin Rusli
Mobile: +6017-6609745
E-mail Address: shahrizalr@utm.my
Nationality: Malaysian

B. ACADEMIC QUALIFICATIONS

June 2016	PhD in Electrical Engineering *Thesis Title: Run-Time Transmission Reconfigurable Power and Adaptive Packet Relocator for Wireless Network-on-Chip* Research Laboratory: VLSI & Embedded Computing Architecture Design (VeCAD) Department: Electronic and Computer Engineering, Universiti Teknologi Malaysia (UTM)
Oct 2010	M.Eng (Electrical – Electronic & Telecommunications) - UTM.
July 2006	B.Eng (Computer) (Hons) - UTM.

C. WORK EXPERIENCES

June 2016 – present	Senior Lecturer at UTM Faculty of Artificial Intelligence (present) Faculty of Electrical Engineering (2007-2024)
May 2021 – October 2023	Senior Physical Design System-on-Chip Engineer at Mediatek (Singapore) Pte Ltd (Industry Attachment)
June 2019 – August 2019	Visiting Lecturer at Intel Technology (Malaysia), Penang
June 2014 – Aug 2015	Research Attachment at University of Catania, Italy and University of California Irvine, USA
Oct 2007 – May 2016	Tutor at UTM
August 2006 – Sept 2007	Research Engineer at Centre for Artificial Intelligence and Robotics (CAIRO) UTM

D. PROFESSIONAL MEMBERSHIP

Institute of Electrical and Electronics Engineers (IEEE) – 99204475
The Institution of Engineering and Technology (IET) - 1101114034
Board of Engineers Malaysia (BEM) – 69865A
Malaysian Simulation Society (MSS) – 0019

E. TEACHING ACTIVITIES

Postgraduate Courses
(2024) : Embedded System Design
(2019 – 2024) : VLSI Design Automation

Undergraduate Courses
(2016 - 2024) : Embedded Processor System
(2018 - 2023) : Microprocessor
(2023 - 2024) : Digital Electronic System
(2017) : Computer Architecture & Organization
(2010) : Basic Electronics

F. HUMAN CAPITAL DEVELOPMENT

Postgraduate

PhD / Doctoral

1. (On-going) Nur Afiqah Ab Razak, "Communication Modelling in Neuromorphic Computing". Supervisor.
2. (On-going) Md Sabbir Hossain Sajib, "Cache Coherence for High-Speed Memory in Artificial Intelligence Chip". Supervisor.
3. (On-going) Zhou Deyang, "Transformer-Based Reinforcement Learning for Cooperative Multi-Agent Systems". Supervisor.
4. (On-going) Ibrahim Yousef M Al-Shareef, "Spatial Convolutional Neural Network". Co-supervisor.
5. (2023) Ayodeji Ireti Fasiku, "Traffic-Aware Medium Access Mechanism for Wireless Network-on-Chip". Co-supervisor. Graduated.
6. (2022) Asrani Lit, "Bidirectional MAC with Congestion-Aware Mechanism for Wireless Network-on-Chip". Co-supervisor. Graduated.

Master

1. (On-going) Nik Muhammad Afif Nik Rumzi, "Machine Learning Based Engineering Change Order for Integrated Circuit Physical Design," Supervisor.
2. (On-going) Jaiganesh Thevadas, "Artificial Intelligence Model for Efficient Machine Vision Inspection of Chip Defects," Supervisor.
3. (2024) Ashraf Aminin Arman Alim "Hardware Accelerator for Matrix Processing on FPGA," Supervisor.
4. (2024) Izzat Idris "Enhancing Timing Engineering Change Order Under Multiple Corners Using Machine Learning Optimizations," Supervisor.
5. (2020) Amanda Thiah Su Lin, "Support Vector Machine Hardware Accelerator for Tongue Color Diagnosis," Supervisor.
6. (2020) Loh Shu Ting, "Hardware Accelerator Implementation of Colour Correction Algorithm," Supervisor.
7. (2020) Tan Yi Chen, "Tongue Colour Diagnosis System Using Convolutional Neural Network," Supervisor.
8. (2020) Mohammed Isam Eldin Hasan Mohammed, "FPGA Based Convolutional Neural Network Hardware Accelerator with Optimized Memory Architecture," Supervisor.

Bachelor

1. (2024) Teo Jun Long, "Real-Time Thermal Management System Monitoring for Electric Vehicle Battery"
2. (2024) Lim Jia Hoe, "Critical Path Prediction Module for Fast Static Timing Analysis"
3. (2024) Lui Shi Shi, "Low Power Memory Controller for Memory Design"
4. (2023) Harith Wafi Mohd Rosman, "Engineering Change Order Synthesis of Gate Level Netlist"
5. (2023) Sam Man Lung, "Machine Learning Based Engineering Change Order for Integrated Circuit Sign-Off"
6. (2023) Chai Bing Cheng, "Universal Asynchronous Receiver and Transmitter and Serial Peripheral Interface Controller Design on FPGA"
7. (2020) Muhammad Arif Hakimi Zamrai, "ASIC Implementation of Advanced Encryption Standard with Clock Gating Technique"
8. (2020) Victor Lee Hao Chuan, "ASIC Implementation of Present Encryption Algorithm with Low Power Technique"
9. (2019) Chin Hung Vui, "Real Time Hand Gesture Recognition Using Deep Learning for Smart Home System", Innovate Malaysia Design Competition
10. (2018) Lim Ji Chen, Chin Linn Kern, Matthias Tiong Foh Thye, Intelligent CCTV for Workplace Safety and Security Using TensorFlow Deep Learning Application, The Excellence Award in 2018 Innovate Malaysia Design Competition.

G. RESEARCH COLLABORATION AND DEVELOPMENT

On-going Projects

1. UTM Flagship CoE / RG Grant
   Title: High-performance Cache Coherence Network-on-chip for Artificial Intelligence System-on-Chip.
2. Title: Battery Management System System-on-Chip for Electric Vehicle
3. Title: Prototype Development of AI-on FPGA Platform for Health Application

Past Projects

1. International Industry Grant, 2022 – Krakatoa Technologies Pte Ltd (Singapore)
   Title: Design Space Exploration of RISC-V Core with Hybrid Interconnects
2. UTM Research University Grant (RUG), 2019
   Title: Traffic Flows Classification Using Machine Learning Techniques to Control Children's Activity
3. UTM Research University Grant (RUG), 2019
   Title: Traffic-Aware Medium Access Mechanism for Wireless Network-on-Chip
4. UTM Research University Grant (RUG), 2019
   Title: Privacy Enhancement of Anonymous Reputation Algorithm in Participatory Crowdsensing
5. Malaysia Ministry of Education - Prototype Research Grant Scheme (PRGS), 2019.
   Title: Development of Embedded Systems Platform Using AMIR CPU
6. UTM Research University Grant (RUG), 2017
   Title: Hybrid Reconfigurable Transmitting Power and Adaptive Packet Relocator Scheme in Wireless Network-on-Chip
7. UTM Research University Grant (RUG), 2017
   Title: ASIC Design of an Energy Efficient Two-dimensional Discrete Cosine Transform

H. PUBLICATIONS

Web of Science

1. **Mohd Shahrizal Rusli**, Asrani Lit, Muhammad Nadzir Marsono, Ab Al-Hadi Ab Rahman, Shahidatul Sadiah, Michael Tan Loong Peng, Suhaila Isaak, Norlina Paraman, 2025. DA+BMAC: Distance-Aware Bidirectional Medium Access Control for Mesh Wireless Network-on-Chip *(Accepted for publication, to appear in IEEE Access)*, **Q2**
2. Nuzhat Khan, Ab Al-Hadi Ab Rahman, Shahriyar Masud Rizvi, Muhammad Nadzir Marsono, Muhammad Paend Bakht, **Mohd Shahrizal Rusli,** Shahidatul Sadiah, 2025. Systematic Literature Review of Machine Learning Models and Application for Text Recognition *(Accepted for publication, to appear in IEEE Access)*, **Q2**
3. Chuan, M.W., Wong, K.L., Hamzah, A., **Rusli, S**., Alias, N.E., Lim, C.S. and Tan, M.L., 2020. 2D honeycomb silicon: A review on theoretical advances for silicene field-effect transistors. Current Nanoscience, 16(4), pp.595-607, **Q2**
4. Chuan, M.W., Wong, K.L., Hamzah, A., **Rusli, S**., Alias, N.E., Lim, C.S. and Tan, M.L.P., 2020. A review of the top of the barrier nanotransistor models for semiconductor nanomaterials. Superlattices and Microstructures, 140, p.106429, **Q2**
5. Chuan, M.W., Wong, K.L., Hamzah, A., **Rusli, S**., Alias, N.E., Lim, C.S. and Tan, M.L.P., 2020. Electronic properties and carrier transport properties of low-dimensional aluminium doped silicene nanostructure. Physica E: Low-dimensional Systems and Nanostructures, 116, p.113731, **Q2**
6. Wong, K.L., Chuan, M.W., Hamzah, A., **Rusli, S**., Alias, N.E., Sultan, S.M., Lim, C.S. and Tan, M.L.P., 2020. Performance metrics of current transport in pristine graphene nanoribbon field-effect transistors using recursive non-equilibrium Green's function approach. Superlattices and Microstructures, 145, p.106624, **Q2**
7. Kamarudin, N.D., **Rusli, M.S**., Yee, O.C., Mansoor, S.B.R.S., Azahari, A.M., Zainol, Z., Abd Ghani, K. and Makhtar, S.N., 2018. Performance Comparison of Colour Correction and Colour Grading Algorithm for Medical Imaging Applications. International Journal of Engineering & Technology, 7(4.33), pp.353-356.
8. **Rusli, M.S.**, Lit, A, Marsono MN, Palesi, M., Adaptive Packet Relocator in Wireless Network-on-Chip (WiNoC), Communications in Computer and Information Science. Springer. Aug 2017. pp. 719-735 ISBN: 18650929.

Scopus

1. Nuzhat Khan, Joyce Ng Ting Ming, Ab Al-Hadi Ab Rahman, Shahidatul Sadiah, **Mohd Shahrizal Rusli**, Muhammad Paend, 2025. Wirelength estimation for VLSI cell placement using hybrid statistical learning. *(Accepted for publication, to appear in Indonesian Journal of Electrical Engineering and Computer Science).*
2. Alshareef, I.Y., Ab Rahman, A.A.H., Khan, N., Rizvi, S.M., Manzak, A., **Rusli, M.S.**, Mohammed, M.S. and Hassan, M.K., 2025. Lightweight and high-precision spectral convolutional neural network model for custom 94-class ASCII character recognition. Neural Computing and Applications, pp.1-22.
3. Loh, S.T., **Rusli, M.S.**, Marsono, M.N., Rahman, A.A.H.A., Paraman, N., Sadiah, S., Tan, M.L.P., Kamisian, I., Pusppanathan, J. and Kamarudin, N.D., 2024, December. Hardware Accelerator Simulation for Colour Correction Algorithm. In International Symposium on Systems Modelling and Simulation (pp. 295-307). Singapore: Springer Nature Singapore.

4. Awab, A.H., Ab Rahman, A.A.H., **Rusli, M.S**., Sheikh, U.U., Kamisian, I. and Meng, G.K., 2019. HEVC 2D-DCT architectures comparison for FPGA and ASIC implementations. TELKOMNIKA (Telecommunication Computing Electronics and Control), 17(5), pp.2457-2464.
5. Ney, H.W., Ab Rahman, A.A.H., Awab, A.H., **Rusli, M.S**., Sheikh, U.U. and Meng, G.K., 2019. Hardware design of a scalable and fast 2-D hadamard transform for HEVC video encoder. Indonesian Journal of Electrical Engineering and Computer Science, 15(3), pp.1401-1410.
6. Wong, K.L., Chuan, M.W., Chong, W.K., Hamzah, A., **Rusli, M.S.B.,** Alias, N.E.B., Lim, C.S. and Tan, M., 2019. Influence of single vacancy defect at varying length on electronic properties of zigzag graphene nanoribbons. Indonesian Journal of Electrical Engineering and Informatics (IJEEI), 7(2), pp.366-374.
7. **M. S. Rusli**, A. A. H. Ab Rahman, U. U. Sheikh, N. Shaikh Husin, Michael L. P. Tan, T. Andromeda, M. N. Marsono, Performance Evaluation of Centralized Reconfigurable Transmitting Power Scheme in Wireless Network-on-Chip. Telecommunication, Computing, Electronics and Control (TELKOMNIKA), 2018. Vol. 16(6). pp. 2844-2854.
8. **M.S. Rusli**, N.D. Kamarudin, A. A. H. Ab Rahman, M. N. Marsono, Evaluation of Scheme Selection and Parameter Effects in the Reconfigurable Transmitting Power in Wireless Network-on-Chip. Science & Technology Research Institute for Defence (STRIDE), 2018. Vol. 181. pp. 170–180.
9. Kamarudin, N.D., Rahayu, S.B., Zainol, Z., **Rusli, M.S**. and Ghani, K.A., 2018. Performance comparison of machine learning classifiers on aircraft databases. Science & Technology Research Institute for Defence (STRIDE) (1985–6571), 11(2), pp.154-169.
10. **Rusli, M.S.**, Mineo, A., Palesi, M., Ascia, G., Catania, V., Yee, O.C. and Marsono, M.N., 2015. A closed Loop Power Manager for Transmission Power Control in Wireless Network-on-Chip Architectures. Jurnal Teknologi (Sciences & Engineering), 75(1). DOI: https://doi.org/10.11113/jt.v75.3813.

Proceedings

1. Radzri, M.L.M., Paraman, N. and **Rusli, M.S**., 2023, October. ASIC Implementation for Multiple Scan at Register Transfer Level. In Journal of Physics: Conference Series (Vol. 2622, No. 1, p. 012026). IOP Publishing.
2. Ahmadi, A., Paraman, N., **Rusli, M.S**. and Isaak, S., 2023, May. Hybrid non scan with built-in self-test for fault coverage improvement. In AIP Conference Proceedings (Vol. 2795, No. 1). AIP Publishing.
3. Sadiah, S., Chun, L.J., Ismail, I., **Rusli, M.S**. and Syafiq, M.U., 2023, May. High-throughput and low-latency ASIC implementation of lightweight cryptography. In AIP Conference Proceedings (Vol. 2795, No. 1). AIP Publishing.
4. Tan, Y.C., **Rusli, M.S**., Kamarudin, N.D., Ab Rahman, A.A.H., Sheikh, U.U.S.I.U., Tan, M.L.P. and Shapiai, M.I., 2022, August. Tongue Colour Diagnosis System Using Convolutional Neural Network. In Journal of Physics: Conference Series (Vol. 2319, No. 1, p. 012033). IOP Publishing.
5. Awab, A.H., Rahman, A.A.H.A., Kamisian, I. and **Rusli, M.S**., 2021. VLSI Design of a Split Parallel Two-Dimensional HEVC Transform. In Innovations in Electrical and Electronic Engineering: Proceedings of ICEEE 2021 (pp. 431-440). Springer Singapore.
6. Latib, N.A.A., Rahman, A.A.H.A. and **Rusli, M.S**., 2021. Design and Implementation of Bluetooth Low Energy Link Layer Controller Using Dataflow Programming. In Innovations in Electrical and Electronic Engineering: Proceedings of ICEEE 2021 (pp. 593-604). Springer Singapore.
7. Al-Hchaimi, A.A.J., Flayyih, W.N., Hashim, F., **Rusli, M.S**. and Rokhani, F.Z., 2021, November. Review of 3D networks-on-chip simulators and plugins. In 2021 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia) (pp. 17-20). IEEE.
8. Fasiku, A.I., Oladokun, O., **Rusli, S**. and Marsono, M.N., 2021, June. A Centralized Token-based Medium Access Control Mechanism for Wireless Network-on-Chip. In 2021 International Conference on Artificial Intelligence and Computer Science Technology (ICAICST) (pp. 102-107). IEEE.
9. Chuan, M.W., Wong, K.L., Hamzah, A., **Rusli, S**., Alias, N.E., Lim, C.S. and Tan, M.L.P., 2020, July. Device performance of silicene nanoribbon field-effect transistor under ballistic transport. In 2020 IEEE International Conference on Semiconductor Electronics (ICSE) (pp. 5-8). IEEE.
10. Fasiku, A.I., **Rusli, S**. and Marsono, M.N.B., 2020, September. Characterization of subnets, virtual channel and routing on wireless network-on-chip performance. In 2020 IEEE Student Conference on Research and Development (SCOReD) (pp. 117-121). IEEE.
11. Mineo, A., **Rusli, M.S.**, Palesi, M., Ascia, G., Catania, V. and Marsono, MN., A Closed Loop Transmitting Power Self-Calibration Scheme for Energy Efficient WiNoC Architectures, Proc. IEEE/ACM Design, Automation & Test in Europe Conference and Exhibition (DATE 2015). Grenoble, France. 2015. pp. 513-518.

12. **Rusli, M.S**., Mineo, A., Palesi, M., Ascia, G., Catania, V. and Marsono, MN., A Closed Loop Control Based Power Manager for WiNoC Architectures. Proc ACM International Workshop on Manycore Embedded Systems. (MES 2014). Minneapolis, USA. 2014. pp. 60-63.

I. PROFESSIONAL SERVICES

1. Certified HRDF Trainer for microcredential course: Chip Layout: Partitioning & Floorplanning Automation - 2024
2. Certified HRDF Trainer for microcredential course: Chip Layout: Placement & Routing (I) Automation - 2024
3. Certified HRDF Trainer for microcredential course: Chip Layout: Routing (II) Automation to Timing Closure - 2024
4. Postgraduate Coordinator – UTM MEng (Computer and Microelectronic Systems), 2018 – 2021.
5. International IEEE Reviewer – IEEE journals and IEEE conferences, 2016 – 2023.
6. International IEEE conferences executive committee (IEEE Asia Test Symposium, 2018 & IEEE Artificial Intelligence for Sustainable Innovation, 2025).
7. Intel-Elite Internship Committee, Intel Malaysia (2019 - 2024).